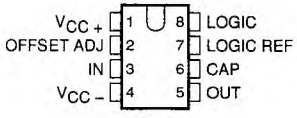
Contents

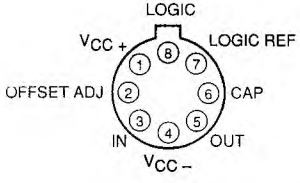
D3218, JULY 1988 – REVISED MARCH 1989

- **Acquisition Time . . . 4 μs Typ**
- **Gain Error . . . 0.01% Max, 0.001% Typ for LF198A, LF398A**
- **Input Offset Voltage . . . 1 mV Max for LF198A, 2 mV Max for LF398A**
- **Hold Step . . . 1 mV Max for LF198A, LF398A**
- **Very Low Feedthrough Attenuation Ratio at f = 1 kHz . . . 96 dB Typ**
- **High Input Impedance . . . 10^{10} Ω Typ**
- **Logic Inputs Compatible With All Logic Families**

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



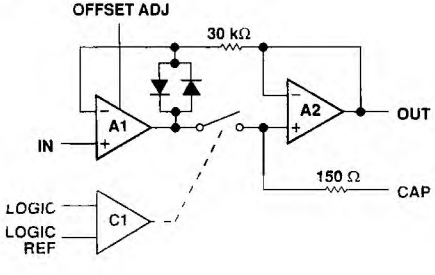
description

These sample-and-hold amplifiers use a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. Input offset voltages as low as 1 mV (LF198A) and gain errors as low as 0.001% (LF198A, LF398A) allow these amplifiers to be used in 12-bit systems. Properly selecting the external hold capacitor optimizes the dynamic performance. Acquisition times can be as low as 4 μs for small capacitors, while hold step and droop errors can be held below 0.1 mV and 30 μV/s, respectively, when using larger capacitors.

The LF198 and LF398 are fixed at unity gain with 10^{10}-Ω input impedance independent of the sample or hold mode. The logic inputs are at a high differential impedance to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the input offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The devices operate over a wide supply voltage range from ±5 V to ±18 V with very little change in performance. Key parameters are specified over this full supply range.

The LF198 and LF198A are characterized for operation over the full military temperature range of –55°C to 125°C. The LF398 and LF398A are characterized for operation from 0°C to 70°C.

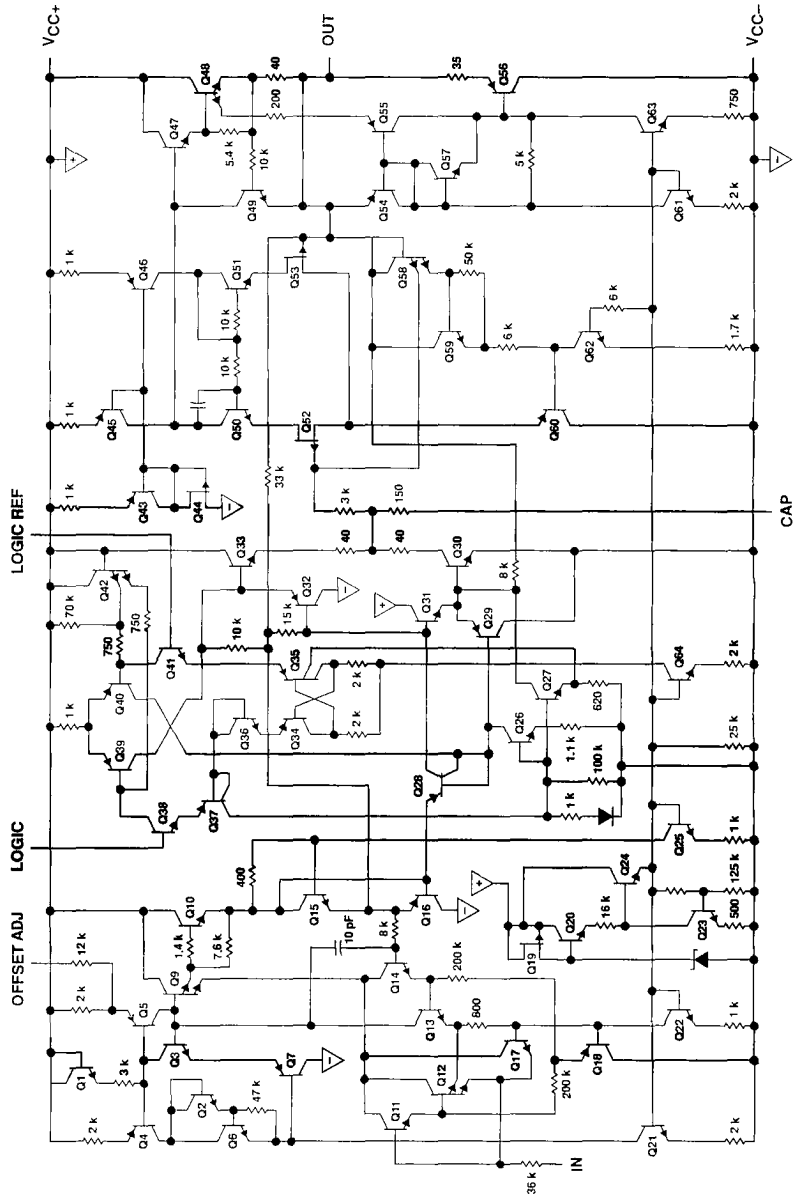
functional block diagram



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE		
		CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	2 mV	—	LF398AL	LF398AP
	7 mV	LF398G	LF398L	LF398P
–55°C to 125°C	1 mV	—	LF198AL	—
	3 mV	—	LF198L	—

schematic



All resistor values shown are nominal and in ohms.

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definition of terms

Acquisition Time
The time required to acquire, within a defined error, a new analog input voltage with an output change of 10 V. Acquisition time includes output settling time and includes the time required for all internal nodes to settle so that the output is at the proper value when switched to the hold mode.

Aperture Time
The delay required between a hold command and an input analog transition so that the transition does not affect the held output.

Dynamic Sampling Error
The error introduced into the held output voltage due to a changing analog input at the time the hold command is given. Dynamic sampling error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error
The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time
The time required for the output to settle within 1 mV of final value after a hold command is initiated.

Hold Step
The voltage step at the output of the amplifier when switching from sample mode to hold mode with a constant analog input voltage and a logic swing of 5 V.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −18 V
Input voltage range, V_I (any input, see Note 1) . . . . . $V_{CC\pm}$
Differential input voltage, logic to logic reference (see Note 2) . . . . . ±30 V
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Duration of hold capacitor short-circuit current . . . . . 10 s
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: LF198, LF198A . . . . . −55°C to 125°C
LF398, LF398A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The logic inputs are protected to ±30 V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both the logic and logic reference pins must be at least 2 V below the positive supply, and one of these pins must be at least 3 V above the negative supply.
3. The output may be shorted to either supply.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR	DERATING ABOVE T_A	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
JG (LF198_)	500 mW	8.4 mW/°C	90°C	500 mW	210 mW
JG (LF398_)	500 mW	6.6 mW/°C	74°C	500 mW	N/A
L (LF198_)	500 mW	6.6 mW/°C	74°C	500 mW	165 mW
L (LF398_)	500 mW	5.2 mW/°C	54°C	416 mW	N/A
P	500 mW	8.0 mW/°C	88°C	500 mW	200 mW

electrical characteristics in sample mode, $V_{CC\pm}$ = ±15 V, V_I = ±11.5 V, C_h = 0.01 µF, R_L = 10 kΩ, logic reference at 0 V, logic at 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LF198			LF398			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±5 V to ±18 V	25°C		1	3		2	7	mV
			Full range			5			10	
I_{IB}	Input bias current		25°C		5	25		10	50	nA
			Full range			75			100	
	Differential logic threshold voltage		25°C	0.8	1.4	2.4	0.8	1.4	2.4	V
	Input current, logic and logic reference		25°C		2	10		2	10	µA
	Leakage current into hold capacitor terminal	$V_{CC\pm}$ = ±5 V to ±18 V, Hold mode, See Note 4	25°C		30	100		30	200	pA
	Hold capacitor charging current	$V_I - V_O$ = 2 V	25°C		5			5		mA
z_i	Input impedance		25°C		10^{10}			10^{10}		Ω
z_o	Output impedance	Hold mode	25°C		0.5	2		0.5	4	Ω
			Full range			4			6	
	Gain error (see Note 5)	R_L = 10 kΩ	25°C		0.002	0.005		0 004	0.01	%
			Full range			0.02			0.02	
	Feedthrough attenuation ratio	f = 1 kHz	25°C	86	96		80	96		dB
	Hold step (see Note 6)	V_O = 0	25°C		0.5	2		0.5	2.5	mV
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ±5V to ±18 V, V_O = 0	25°C	80	110		80	110		V
I_{CC}	Supply current	$V_{CC\pm}$ = ±5 V to ±18 V, $T_A \geq 25°C$	25°C		4.5	5.5		4.5	6.5	mA
	Acquisition time to 0.1% (see Note 5)	ΔV_O = 10 V, C_h = 1 µF	25°C		4			4		µs
		ΔV_O = 10 V, C_h = 0.01 µF			16			16		

†Full range is −55°C to 125°C for the LF198 and 0°C to 70°C for the LF398.

NOTES: 4. The effects of a rise in junction temperature due to power dissipation or elevated ambient free-air temperature can be approximated by doubling the 25°C value for each 11°C increase in junction temperature. The specified limit applies for the full input signal range.
5. See definition of terms.
6. See definition of terms. Hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. Stray capacitance of 1 pF, for example, creates an additional 0.5-mV step with a 5-V logic swing and a 0.01-µF hold capacitor. The magnitude of the hold step is inversely proportional to the value of the hold capacitor.

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electrical characteristics in sample mode, $V_{CC\pm}$ = ±15 V, V_I = ±11.5 V, C_h = 0.01 µF, R_L = 10 kΩ, logic reference at 0 V, logic at 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LF198A			LF398A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±5 V to ±18 V	25°C		0.5	1		1	2	mV
			Full range			2			3	
I_{IB}	Input bias current		25°C		5	25		10	25	nA
			Full range			75			50	
	Differential logic threshold voltage		25°C	0.8	1.4	2.4	0.8	1.4	2.4	V
	Input current, logic and logic reference		25°C		2	10		2	10	µA
	Leakage current into hold capacitor terminal	$V_{CC\pm}$ = ±5 V to ±18 V, Hold mode, See Note 4	25°C		10	100		10	100	pA
	Hold capacitor charging current	$V_I - V_O$ = 2 V	25°C		5			5		mA
z_i	Input impedance		25°C		10^{10}			10^{10}		Ω
z_o	Output impedance	Hold mode	25°C		0.5	1		0.5	1	Ω
			Full range			4			6	
	Gain error (see Note 5)	R_L = 10 kΩ	25°C		0.001	0.005		0.001	0.005	%
			Full range			0.01			0.01	
	Feedthrough attenuation ratio	f = 1 kHz	25°C	86	96		86	96		dB
	Hold step (see Note 6)	V_O = 0	25°C		0.25	1		0.25	1	mV
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ±5 V to ±18 V, V_O = 0	25°C	90	110		90	110		V
I_{CC}	Supply current	$V_{CC\pm}$ = ±5 V to ±18 V, $T_A \geq 25°C$	25°C		4.5	5.5		4.5	6.5	mA
	Acquisition time to 0.1% (see Note 5)	ΔV_O = 10 V, C_h = 1 µF	25°C		4	6		4	6	µs
		ΔV_O = 10 V, C_h = 0.01 µF			16	25		16	25	

†Full range is −55°C to 125°C for the LF198A and 0°C to 70°C for the LF398A.

NOTES: 4. The effects of a rise in junction temperature due to power dissipation or elevated ambient free-air temperature can be approximated by doubling the 25°C value for each 11°C increase in junction temperature. The specified limit applies for the full input signal range.
5. See definition of terms.
6. See definition of terms. Hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. Stray capacitance of 1 pF, for example, creates an additional 0.5-mV step with a 5-V logic swing and a 0.01-µF hold capacitor. The magnitude of the hold step is inversely proportional to the value of the hold capacitor.

TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

INPUT BIAS CURRENT
vs
JUNCTION TEMPERATURE

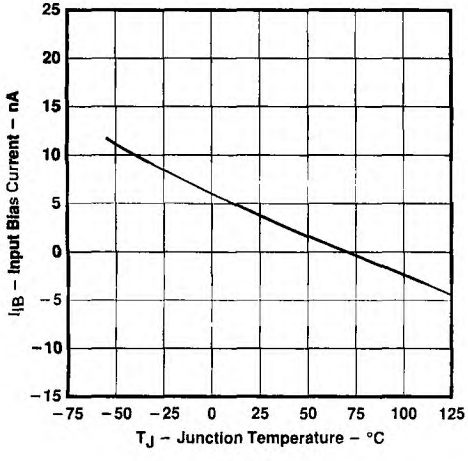

FIGURE 1

LF198A, LF398A
CAPACITOR TERMINAL LEAKAGE CURRENT
vs
JUNCTION TEMPERATURE

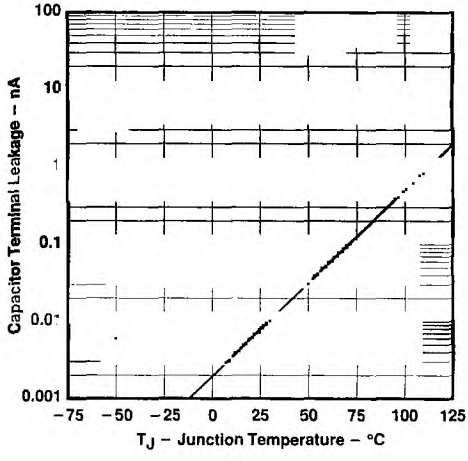

FIGURE 2

GAIN ERROR

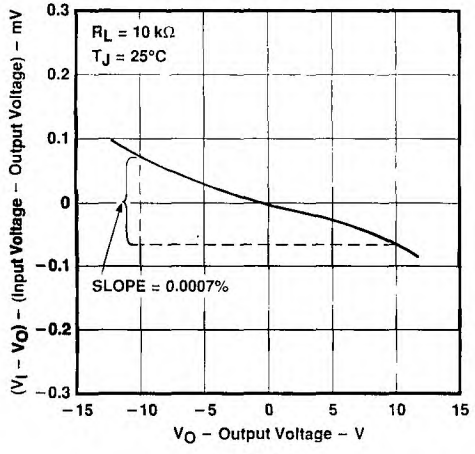

FIGURE 3

FEEDTHROUGH ATTENUATION RATIO
vs
FREQUENCY

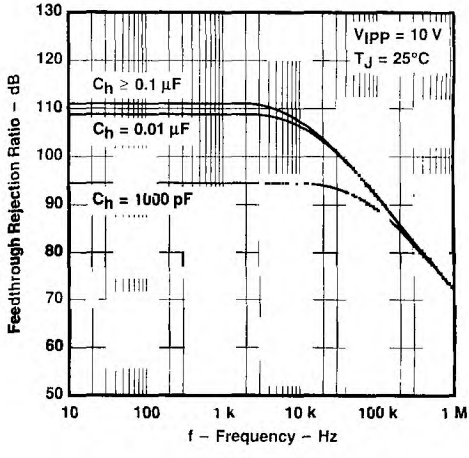

FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

HOLD STEP
vs
INPUT VOLTAGE

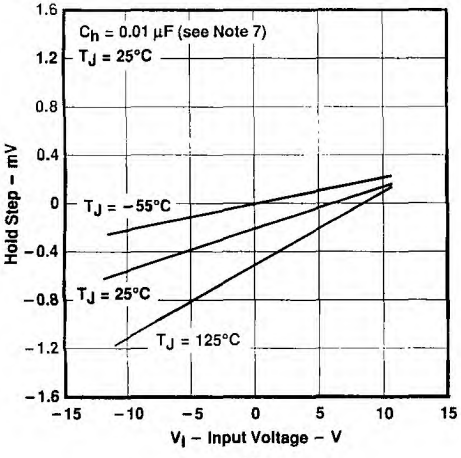

FIGURE 5

HOLD STEP
vs
HOLD CAPACITANCE

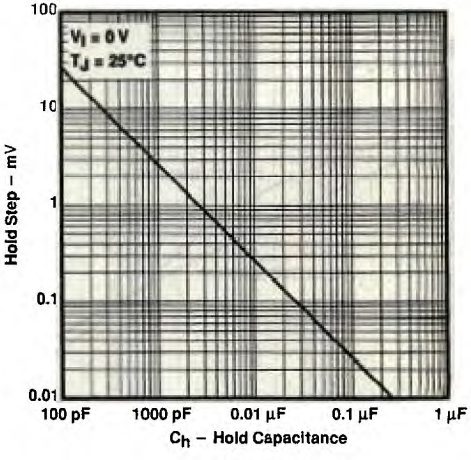

FIGURE 6

HOLD STEP
vs
LOGIC SLEW RATE

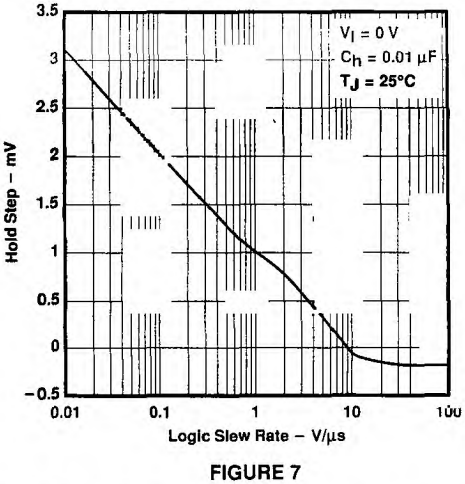

FIGURE 7

SMALL-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION and PHASE DELAY
vs
FREQUENCY

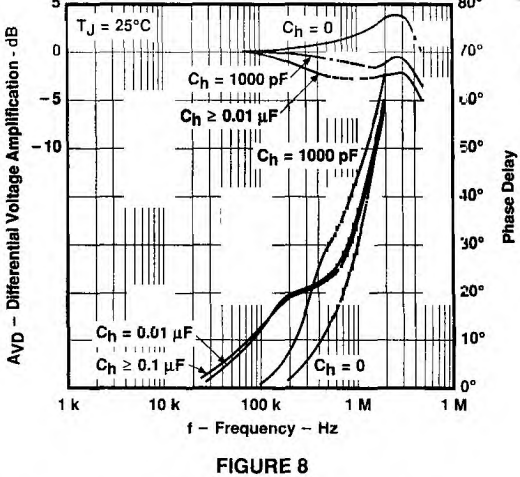

FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 7: The amplitude of the hold step varies inversely with the value of the hold capacitor.

TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

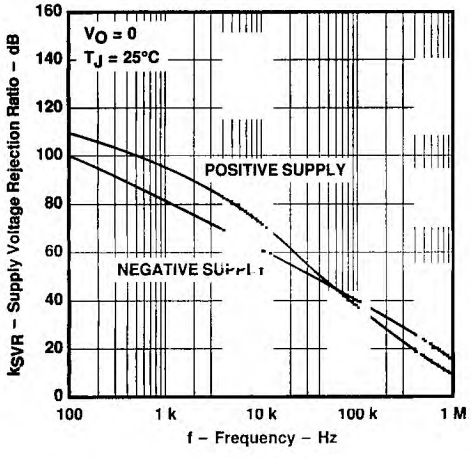

FIGURE 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

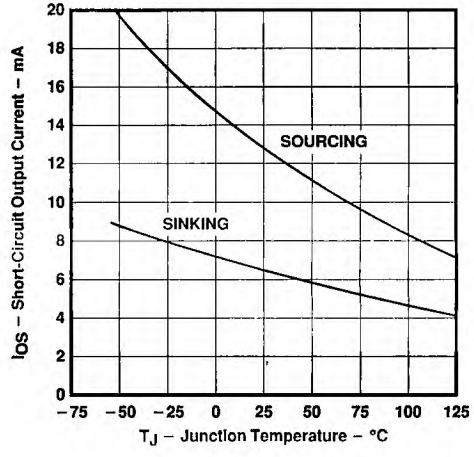

FIGURE 10

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

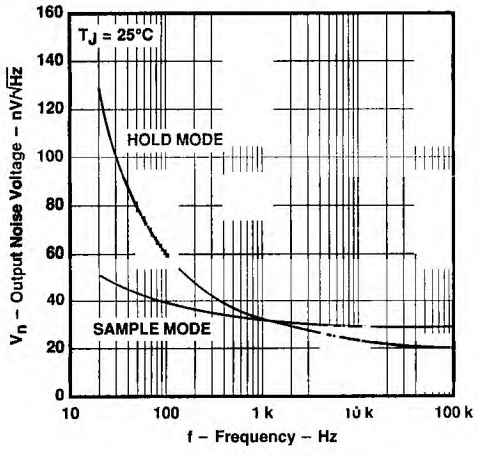

FIGURE 11

DYNAMIC SAMPLING ERROR
vs
INPUT SLEW RATE

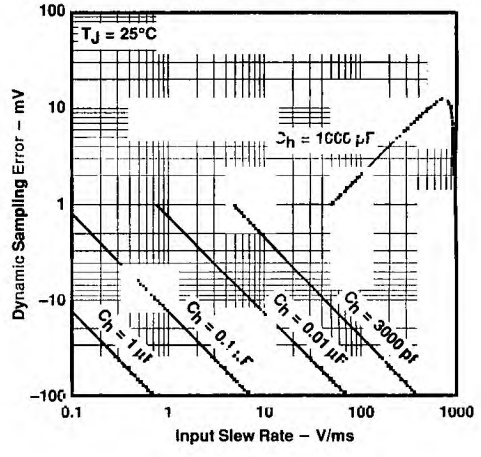

FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

APERTURE TIME
vs
JUNCTION TEMPERATURE

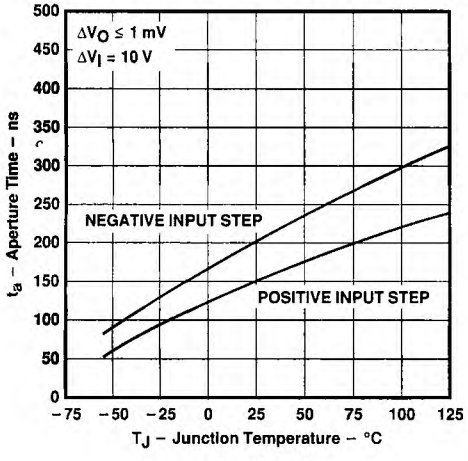

FIGURE 13

HOLD SETTLING TIME
vs
JUNCTION TEMPERATURE

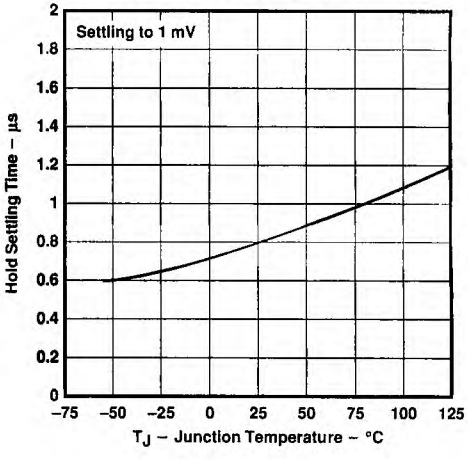

FIGURE 14

ACQUISITION TIME
vs
HOLD CAPACITANCE

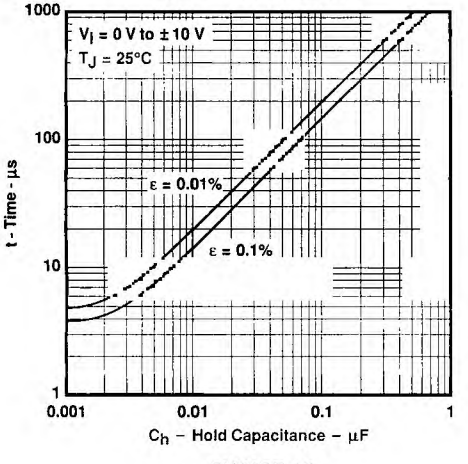

FIGURE 15

OUTPUT DROOP RATE
vs
HOLD CAPACITANCE

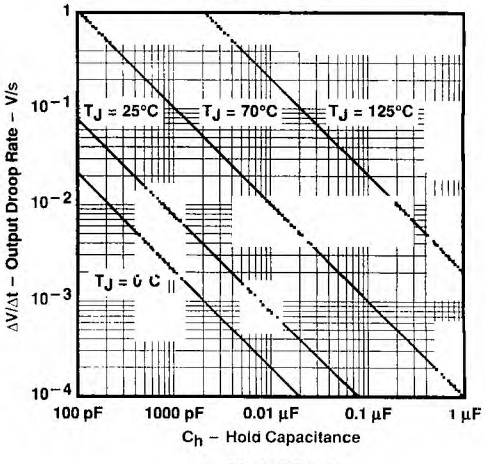

FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

CAPACITOR DIELECTRIC ABSORPTION
vs
SAMPLE TIME

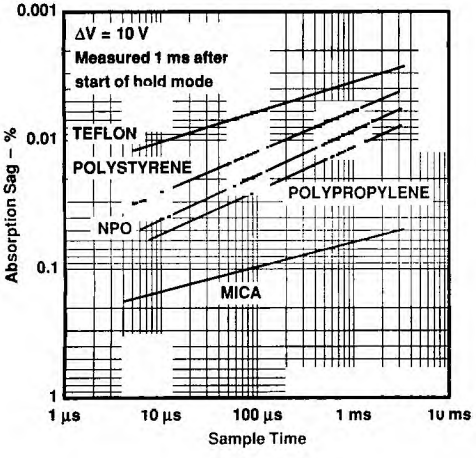

FIGURE 17

CAPACITOR DIELECTRIC ABSORPTION
vs
TIME IN HOLD MODE

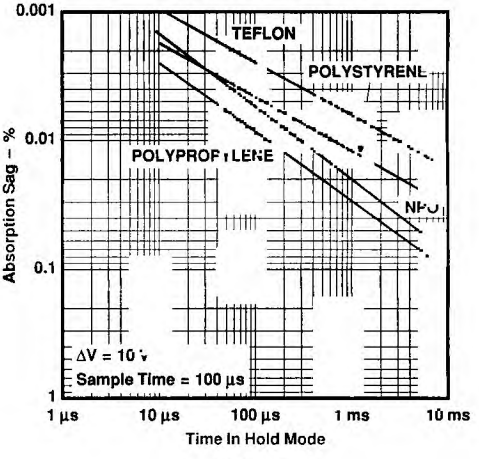

FIGURE 18

OUTPUT TRANSIENT
AT START OF HOLD MODE

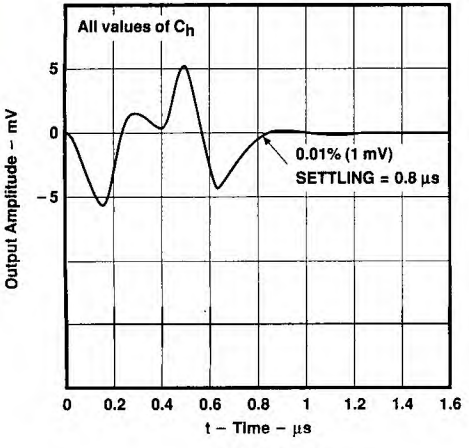

FIGURE 19

OUTPUT TRANSIENT
AT START OF SAMPLE PERIOD

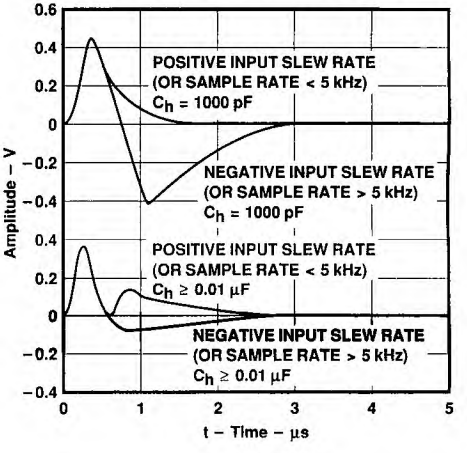

FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

4 Special Functions

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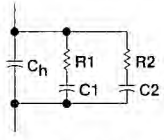
TYPICAL APPLICATION DATA

hold capacitor

For fast sample-and-hold applications, the value of the hold capacitor is critical. A low value gives fast acquisition but also increases errors due to hold step and droop caused by amplifier bias current. The capacitor should be made as large as possible consistent with acquisition time and dynamic sampling error requirements. Capacitors larger than 0.1 μF are generally not available in the low-loss dielectrics like Teflon, Polystyrene, and NPO, at least not at a reasonable price and size. Mylar, even with its poor dielectric absorption properties, may be a reasonable choice when very long sample times are used and low droop rates are needed.

Dielectric absorption in the hold capacitor can often be the major source of error in a sample-and-hold amplifier. The equivalent "circuit" of a typical capacitor with parallel RC networks used to model dielectric absorption is shown in Figure 21. In this capacitor, rapid changes in capacitor voltage are not tracked by the internal parasitic capacitors because of the resistance in series with them. This leads to a "sag" effect in the hold capacitor after a sudden change in voltage followed by a rapid switch to the hold mode. The capacitor remembers its previous state via the charge in the internal parasitic capacitance and sags back slightly toward the previous voltage. The magnitude of the sag depends upon the voltage change and the time spent sampling the new voltage. Several time constants are typically evident in the sag, although some capacitors tend to exhibit a single time constant, while others show a sag that indicates a blending of many time constants. Figures 17 and 18 show the amount of sag found after a 10-V step, with sample time at the new voltage and hold time at the new voltage as variables. It is obvious that sag problems are minimized by long sample times and short hold times. While this is often in conflict with basic sampling requirements, the sample-and-hold amplifier should be kept in the "tracking", or sampling, mode as much as possible to maximize the time the hold capacitor spends near the voltage at which it eventually "holds".



NOTE: C1 and C2 are approximately equal to $0.01C_h$ to $0.1C_h$. R1 and R2 generate time constants of 0.1 to 50 ms with C1 and C2.

FIGURE 21. TYPICAL HOLD CAPACITOR EQUIVALENT CIRCUIT

The best capacitor for sample-and-hold applications is Teflon, which is clearly superior with regard to dielectric absorption and operates over the full temperature range (−55°C to 125°C). If size or price is a problem, the second choice for full-temperature-range operation is NPO (or COG) ceramic units. Some care must be used because not all NPO capacitors use the low-dielectric-constant ceramic necessary for low dielectric absorption. For lower temperature (≤ 70°C), Polystyrene has traditionally been the best hold capacitor. The best units are cylindrical and fairly large; there seems to be a strong correlation between small size and poor dielectric performance. Polypropylene has nearly the same absorption properties as polystyrene and offers 85°C operation; it also tends to be smaller. Other standard dielectrics such as mica, glass, mylar, and ordinary ceramic are much worse with regard to dielectric absorption. Mylar is sometimes used for large values when the ratio of sample to hold time is large and extremely low droop is required.

dynamic sampling error

A significant sampling error can occur in any sample-and-hold amplifier if the input is moving when the unit is put into the hold mode. The two major causes for this error are digital delay in switch opening and analog delay across the hold capacitor. The switch opening delay is obvious and leads to a "held" output error of $(dv/dt) \times t_d$; dv/dt is the slew rate of the input signal and t_d is the switch delay. For this device, t_d is approximately 150 ns, giving a 4.5-mV error when sampling the zero crossing of a 5-V (peak) sine wave at 1 kHz ($dv/dt = A \times 2\pi f = 5 \times 2\pi \times 10^3$). The analog delay is the difference between input signal and capacitor voltage. It is determined by the RC product of the hold capacitor and the effective series resistance, which in this device is about 150 Ω.

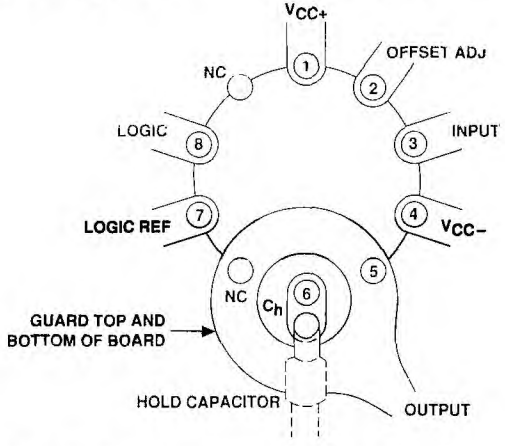
TYPICAL APPLICATION DATA

This analog delay with a 0.01-μF hold capacitor is $R \times C = 150 \times 10^{-8} = 1.5\ \mu s$, or about ten times the delay of the switch. The held output is related in time to the input voltage *before* the hold command was given. The overall dynamic sampling error is the sum of the digital and analog errors. Figure 12 helps estimate these errors as a function of input slew rate and hold capacitor size.

Dynamic sampling error can be reduced by a factor of ten or more by inserting a delay in the logic input so that the "hold" command is delayed by an amount equal to the RC time constant of the device and the external hold capacitor. For a 0.01-μF hold capacitor and the 150-Ω resistor internal to this device, this value is 1.5 μs. A simple RC network can be used in front of the logic input for delays up to approximately 1 μs. Longer delays require the addition of a logic gate to speed up the rise time of the delayed signal. See "logic rise time" for further details.

hold step

Hold step is the small voltage step (after settling) seen at the output of a sample-and-hold amplifier when it is switched from the sample mode to the hold mode with a steady dc input. Hold step is typically the result of, or can be modeled as, a fixed quantity of charge transferred to the hold capacitor due to internal switching that occurs during the hold command. In the case of this device, that charge is approximately 5 pC, giving a hold step of 0.5 mV for a 0.01-μF hold capacitor and 5 mV for a 1000-pF hold capacitor (V = Q/C). Hold step is reasonably independent of logic amplitude if care is taken to minimize the stray capacitance between the logic input and the hold capacitor. With thoughtful layout, including the guarding technique shown in Figure 21, stray capacitance should be under 0.3 pF, limiting charge variations to less than 0.3 pC/V.



NOTE. Use 10-pin layout The guard around C_h is tied to output.

FIGURE 22. GUARDING TECHNIQUE (BOTTOM VIEW)

Hold step varies slightly with analog input voltage (see Typical Characteristics). A typical unit changes at a rate of 0.4 pC/V. This slight variation manifests itself as a gain error when the amplifier is switched to the hold mode. With a 0.01-μF capacitor, the resulting gain error is (0.4 pC/V)/0.01 μF = 0.004%. This gain error is in the opposite direction of dc (sample mode) gain error. When the hold capacitor has a high value, dc gain error dominates and gain is slightly below unity (0.002%). When the hold capacitor has a low value (< 0.01 μF). gain error induced by hold step dominates, and hold-mode gain is slightly above unity. Zeroing out hold step does not change the variation of hold step with regard to input voltage.

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TYPICAL APPLICATION DATA

offset zeroing

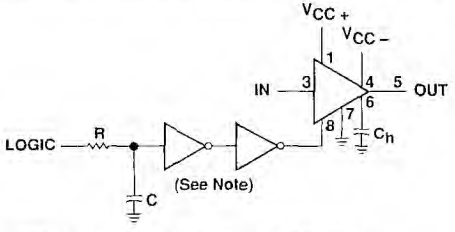
A sample-and-hold amplifier has two distinct offset voltages. The first is the dc offset voltage of the amplifier while in the sample, or "tracking," mode. It is identical to the input offset voltage of any operational amplifier. The second offset voltage is the sum of the dc offset voltage plus a dynamic term called hold step. Hold step is a change in output voltage when the amplifier is switched from sample mode to hold mode with the input held steady. This second offset voltage is often called hold-mode offset voltage. It can be less than or much greater than the dc offset voltage, depending on the magnitude and sign of hold step.

A fairly accurate model for hold step is a fixed charge injected into the hold capacitor by the switch turn-off circuitry. The magnitude of the charge is reasonably independent of logic input amplitude. The resulting change in the hold capacitor is Q/C_h. The charge Q is typically 5 pC, giving a 0.5-mV hold step with a 0.01-μF hold capacitor. Since most sample-and-hold amplifiers are "used" (i.e., have their outputs read by an A-to-D converter), during the hold mode, hold-mode offset voltage is arguably more important than the sample-mode dc offset voltage.

Adjusting dc offset voltage is accomplished with a 1-kΩ low TC cermet potentiometer tied to V_{CC+} with 0.6 mA flowing through it and the wiper tied to pin 2. This allows pin 2 to be moved ± 300 mV around its nominal voltage (0.3 V below V_{CC+}). The offset voltage adjustment range is ± 9 mV, and the adjustment procedure nominally improves offset voltage drift when the dc offset voltage is reduced to zero. This offset method *can* be used to zero out hold-mode offset voltage, but at the expense of some induced offset voltage drift. Each millivolt of hold-step offset corrected by this method introduces 3.3 μV/°C drift. For 0.002-μF hold capacitors or larger with hold step a few millivolts or less, this is a practical solution to hold-mode offset voltage. In precision, wide-temperature-range applications, or when C_h is less than 0.002 μF, a separate hold-mode zeroing method should be used. The circuit shown in Figure 28, which uses a logic inverter and a 5-pF capacitor, is recommended.

logic fall time

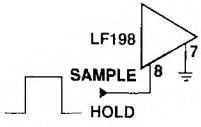
Hold step is independent of logic input fall time only for fall times faster than 10 V/μs. For example, as logic fall time changes from 10 V/μs to 1 V/μs, hold step with a 0.01-μF hold capacitor typically increases from 0.25 mV to 1 mV. (See Figure 7 for more data and refer to Figure 23.) If logic slew rate is not constant, use the value at the threshold point (1.5 V with respect to logic reference). An RC network will have a discharge slew rate of V_L/RC, where V_L is the logic threshold of the LF198. The delay generated by the network will be $RC \times \ln(V_{CC+}/V_L)$, where V_{CC+} is logic amplitude. For a 1-μs delay with 5-V logic , an RC time constant of 0.8 μs is required. This has a slew rate of 2 V/μs at threshold, which slightly degrades hold step. It is obvious that an RC delay network significantly longer than 1 μs will have a large effect on hold step. If longer delays are required, they should be followed by several inverter stages or a Schmitt trigger to increase slew rate.



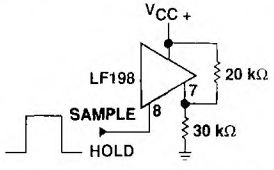
NOTE: Inverters may be eliminated for RC ≤ 3 μs.

FIGURE 23. ADDING DELAY TO LOGIC INPUT

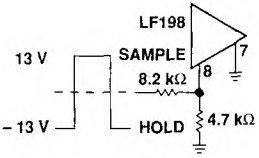
TYPICAL APPLICATION DATA



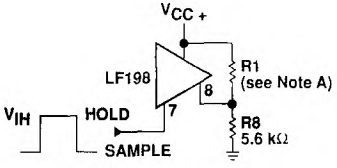
THRESHOLD = 1.4 V



THRESHOLD = $0.6V_{CC+}$ + 1.4 V

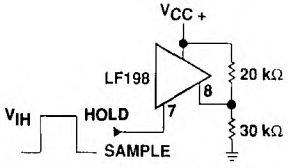


THRESHOLD = 4 V



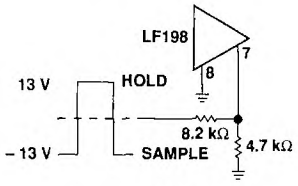
THRESHOLD = 1.4 V

(a) TTL and CMOS
V_{IH} (High State) = 3 V to 10 V



THRESHOLD = $0.6V_{CC+}$ – 1.4 V

(b) CMOS
V_{IH} (High State) = 7 V to 15 V

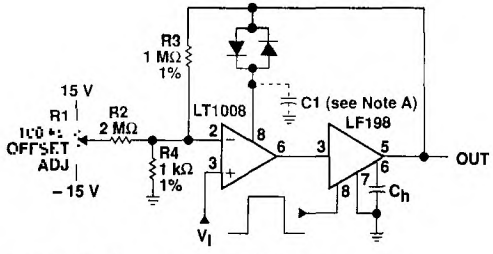


THRESHOLD = – 4 V

(c) OP AMP DRIVE

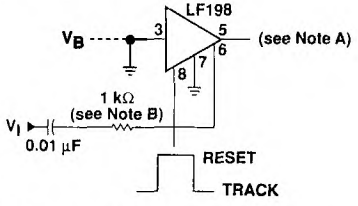
NOTES: A. Select R1 for 2.8 V at pin 8.
B. The logic input signal high level must be at least 2 V below the positive supply voltage of the device.

FIGURE 24. LOGIC INPUT CONFIGURATIONS



NOTE A: For lower gains, the LT1008 must be frequency compensated. Use approximately (100/A_V) pF from comp2 to ground.

FIGURE 25. x1000 SAMPLE-AND-HOLD



NOTES: A. $V_O = V_B + \Delta V_I$ (Hold mode).
B. This resistor protects input from surge currents but increases sample time. It can be eliminated if input is otherwise protected.
C. Output follows input in hold mode and resets to V_B in sample mode.

FIGURE 26. SAMPLE-AND-DIFFERENCE CIRCUIT

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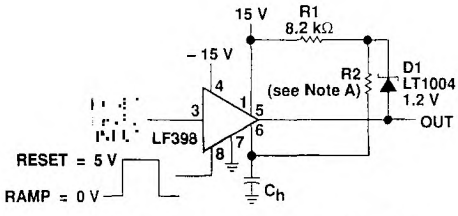
TYPICAL APPLICATION DATA



NOTE A: Select R2 for ramp rate $\Delta V/\Delta t = 1.2\ V/(R2)(C_h)$, $R \geq 10\ k\Omega$.

FIGURE 27. RAMP GENERATOR WITH VARIABLE RESET LEVEL

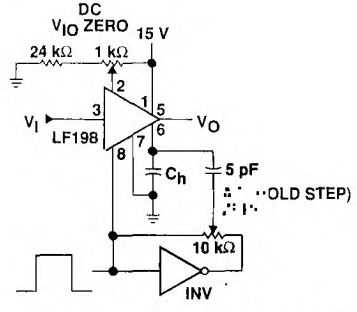
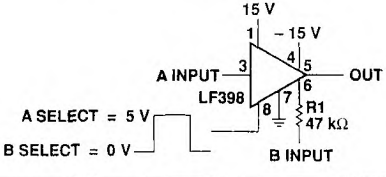
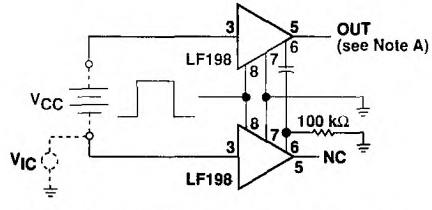


FIGURE 28. DC AND AC ZEROING



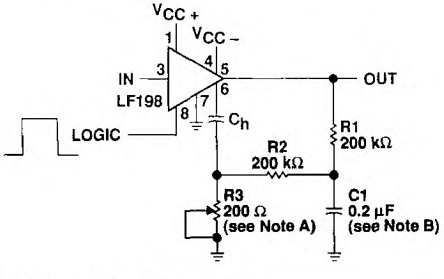
PARAMETER	A	B	UNIT
Gain	1 ± 0.02	1 ± 0.2	%
z_i	10^7	47	kΩ
BW	≈ 1000	≈ 400	kHz
Crosstalk at 1 kHz	– 90	– 90	dB
Offset	≤ 6	≤ 75	mV

FIGURE 29. 2-CHANNEL SWITCH



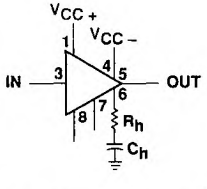
NOTE A: Output equals V_{CC} when in hold mode. Output equals (V_{CC} + V_{IC}) when in sample mode.

FIGURE 30. DIFFERENTIAL HOLD



NOTES: A. Adjust R3 for amplitude.
B. Select for time constant C1 = τ /100 kΩ.

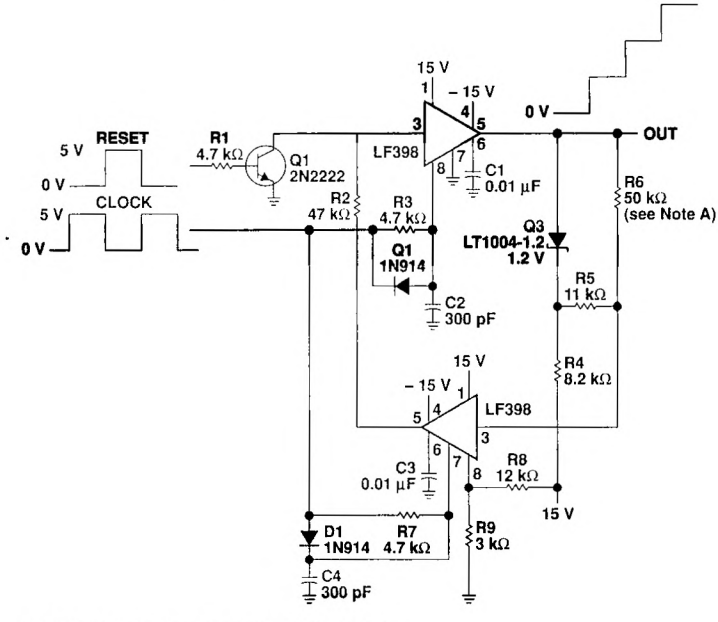
FIGURE 31. CAPACITOR HYSTERESIS COMPENSATION



NOTE A: Select $(R_h)(C_h) >> \frac{1}{2\pi f_{I(MIN)}}$

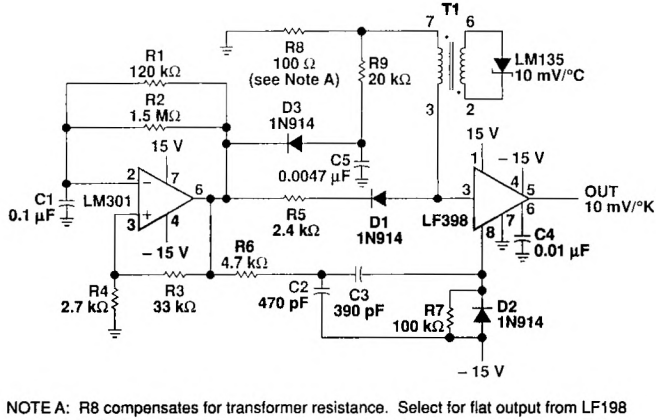
FIGURE 32. OUTPUT HOLDS AT AVERAGE OF SAMPLED INPUT

TYPICAL APPLICATION DATA



NOTE A: Select R6 for step height. 50 kΩ ≈ 1-V step.

FIGURE 33. STAIRCASE GENERATOR



NOTE A: R8 compensates for transformer resistance. Select for flat output from LF198 while in sample mode.

FIGURE 34. ISOLATED TEMPERATURE SENSOR

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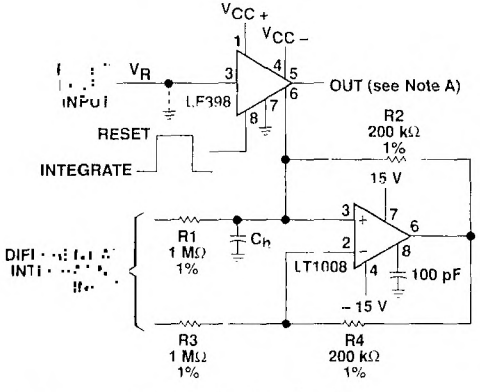
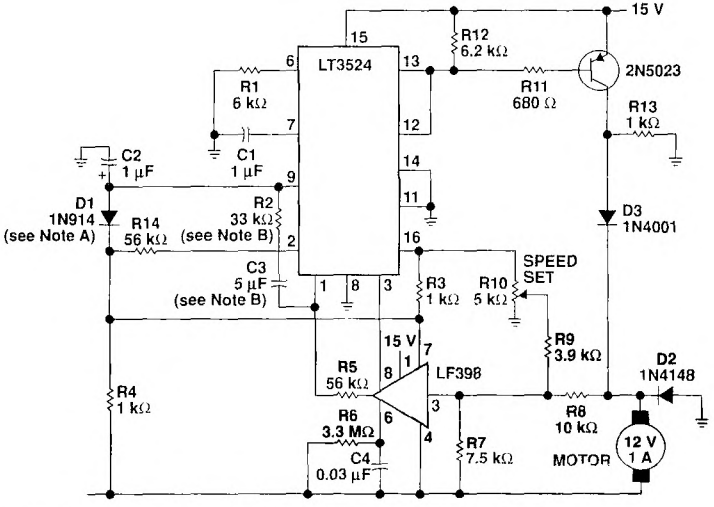
TYPICAL APPLICATION DATA



NOTE A: $V_{O(Hold\ mode)} = \left[\frac{1}{(R1)(C_h)}\int_0^t V_I dt\right] + V_R$

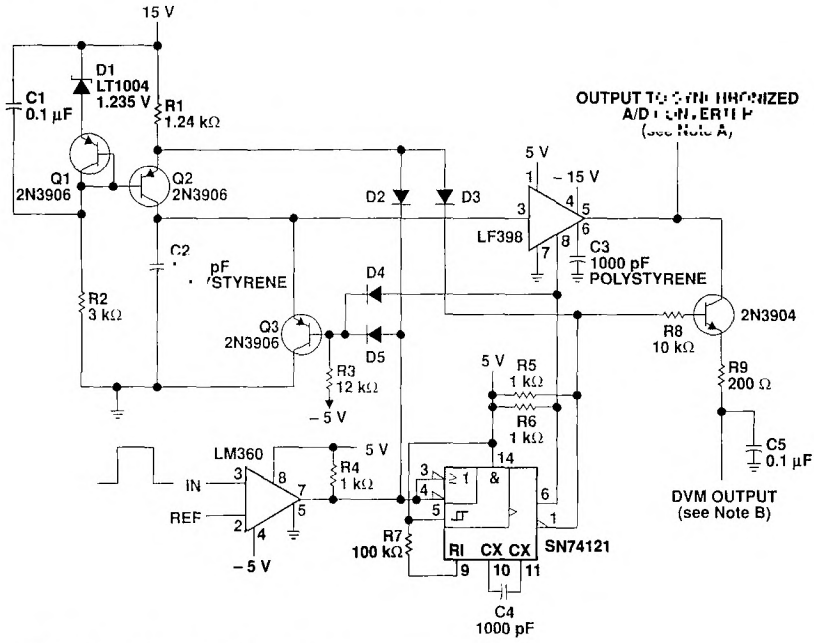
FIGURE 35. INTEGRATOR WITH PROGRAMMABLE RESET LEVEL



NOTES: A. D1 is used for start-up. It limits duty cycle to approximately 75%.
B. Select for optimum loop stability. C3 is nonpolarized.
C. No tachometer is needed; back EMF of motor is sampled and used to control speed.

FIGURE 36. MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA



NOTES: A. Read ≥ 1 µs after Q goes low.
B. For repetitive pulses only. Increase C5 for f ≤ 10 kHz.
C. D2-D5 1N914.

FIGURE 37. PULSE DURATION TO VOLTAGE CONVERTER

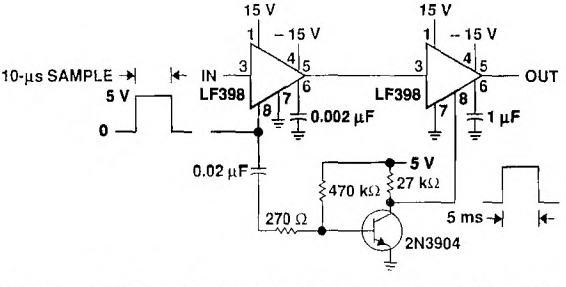


FIGURE 38. FAST-ACQUISITION, LOW-DROOP SAMPLE-AND-HOLD

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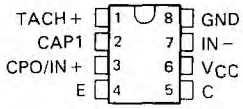
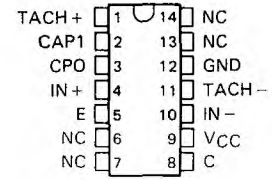
D3003, MARCH • F DC'

- **Output Swings to Ground for Zero-Frequency Input**
- **Only One RC Network Provides Frequency Doubling for Low Ripple**
- **8-Pin Versions Interface Directly to Variable-Reluctance Magnetic Pickups**
- **Uncommitted Collector and Emitter Outputs Provide 40-mA Sink or Source Current to Operate Relays, Solenoids, Meters, or LEDs**
- **Built-In Hysteresis for Noise Immunity**
- **Linearity Typically ±0.3%**
- **8-Pin Versions are Fully Protected from Damage Due to TACH Input Swing Above V_{CC} and Below Ground**

LM2907, LM2917 . . . D OR P PACKAGE
(TOP VIEW)



LM2907, LM2917 . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

applications

Over/under speed sensing
Frequency-to-voltage conversion
Speedometers
Breaker-point dwell meters
Hand-held tachometers
Speed governors
Cruise control
Automotive door-lock control
Clutch control
Horn control
Touch or sound switches

description

The LM2907 and LM2917 are monolithic frequency-to-voltage converters with an output circuit designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The converter (tachometer) section consists of a comparator driving a charge pump and offers frequency doubling for low ripple, full input protection in 8-pin versions, and an output swing to ground for a zero-frequency input. The output section consists of an operational amplifier, normally operating as a comparator, that drives an output transistor with both the collector and emitter floating. The circuit can either sink or source 40 mA of load current.

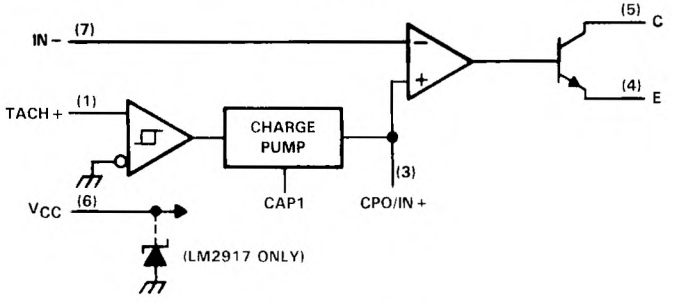
Two basic configurations of the devices are offered; an 8-pin version and a 14-pin version. The 8-pin versions have a ground-referenced tachometer input and an internal connection between the tachometer output and the operational amplifier input. The 8-pin version is well suited to single-speed or single-frequency switching or fully buffered frequency-to-voltage conversion applications. The more versatile 14-pin versions provide differential tachometer inputs and uncommitted operational amplifier inputs. In the 14-pin versions, the tachometer input can be floated and the operational amplifier becomes suitable for active filter conditioning of the tachometer output.

The LM2917 has an active shunt regulator connected across the power leads. The regulator clamps the supply voltage so that stable frequency-to-voltage and frequency-to-current conversions are possible with any supply voltage and a suitable resistor.

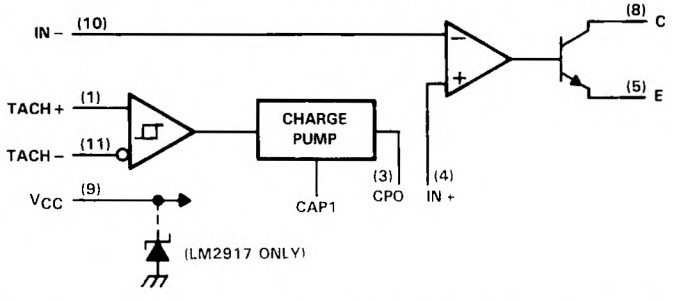
The LM2907 and LM2917 are designed for operation from −40°C to 85°C.

functional block diagrams

8-PIN VERSIONS



14-PIN VERSIONS



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}: LM2907 . . . . . 28 V
Supply current, I_{CC}: LM2917 . . . . . 25 mA
Collector-to-emitter voltage . . . . . 28 V
Operational amplifier input voltage, IN+ and IN– . . . . . 0 V to V_{CC}
Tachometer input voltage: 8-pin version TACH+ . . . . . 0 V to 28 V
14-pin version TACH+ and TACH– . . . . . 0 V to V_{CC}
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperture range 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D (8 pins)	725 mW	5.8 mW/°C	[illegible] mW
D (14 pins)	900 mW	7.2 mW/°C	468 mW
N	1000 mW	7.7 mW/°C	500 mW
P	900 mW	7.2 mW/°C	468 mW

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electrical characteristics, V_{CC} = 12 V (LM2907), V+ = 12 V through 470 Ω (LM2917), T_A = 25°C

converter (tachometer) section

PARAMETER			TEST CONDITIONS	LM2907			LM2917			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_I = 250 mV, f = 1 kHz	±10	±15	±40	±10	±15	±40	mV
V_{hys}	Input hysteresis (see Note 1)		V_I = 250 mV, f = 1 kHz		30			30		mV
V_{IO}	Input offset voltage (see Note 1)	8-pin versions	V_I = 250 mV, f = 1 kHz		5	15		5	15	mV
		14-pin versions	V_{ID} = 250 mV, f = 1 kHz		3.5	10		3.5	10	
I_{IB}	Input bias current		V_I = ±50 mV		0.1	1		0.1	1	μA
V_{OH}	High-level output voltage, CAP1		V_I or V_{ID} = 125 mV		8.3			5.0		V
V_{OL}	Low-level output voltage, CAP1		V_I or V_{ID} = −125 mV		2.3			1.2		V
I_O	Output current, CAP1, CPO		CAP1 and CPO at 6 V	140	180	240				μA
			CAP1 and CPO at 3.8 V				140	180	240	
	Leakage current, CPO		CAP1 open, CPO at 0 V, See Note 3			0.1			0.1	μA
	Gain constant			0.9	1	1.1	0.9	1	1.1	
	Nonlinearity (see Note 2)		f = 1 kHz, 5 kHz, or 10 kHz		0.3	±1		0.3	±1	%

output section

PARAMETER		TEST CONDITIONS	LM2907			LM2917			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_I = 6 V, See Note 3		3	10				mV
		V_I = 3.8 V, See Note 3					3	10	
I_{IB}	Bias current	V_I = 6 V		50	500				nA
		V_I = 3.8 V					50	500	
A_V	Voltage amplification						200		V/mV
I_C	Collector output (sink) current	V_C = 1 V, V_E = 0	40			40	50		mA
I_E	Emitter output (source) current	V_C = V_{CC}, V_E = V_{CC} − 2		−10			−10		mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 5 mA		0.1	0.5		0.1	0.5	V
		I_C = 20 mA			1			1	
		I_C = 50 mA		1	1.5		1	1.5	

NOTES: 1. Hysteresis is the algebraic difference $V_{T+} - V_{T-}$; offset voltage is the difference in magnitudes $|V_{T+}| - |V_{T-}|$. See parameter measurement information test circuits.
2. Nonlinearity is defined as the deviation of V_O at CPO for f = 5 kHz from a straight line defined by the V_O at 1 kHz and V_O at 10 kHz, with C1 = 1000 pF, R1 = 68 kΩ, C2 = 0.22 μF.
3. Pin 2 must be bypassed with a 0.001-μF capacitor to prevent oscillation for these tests.

electrical characteristics

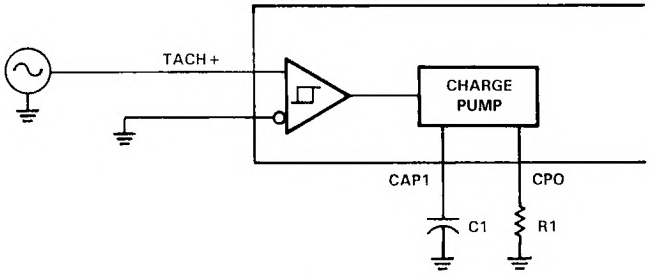
zener regulator (LM2917 only) V+ = 12 V through 470 Ω, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Regulated supply voltage		7.56		V
r_s	Series resistance		10.5	15	Ω
αV_{CC}	Temperature coefficient of regulated supply voltage		1		mV/°C

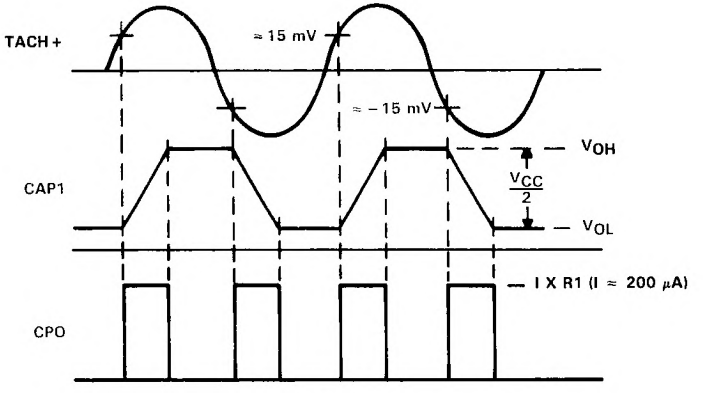
total device (LM2907 only) V_{CC} = 12 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
I_{CC}	Supply current		3.8	6	mA

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

FIGURE 1. TEST CIRCUIT AND WAVEFORMS

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TYPICAL APPLICATION DATA

The LM2907 and LM2917 frequency-to-voltage converter circuits are designed for maximum versatility with a minimum of external parts. The first stage of these devices is a differential comparator. The single-input 8-pin versions have one input grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This version is specifically for magnetic variable-reluctance pickups, which typically provide a single-ended ac output. These single-ended inputs are fully protected against voltage swings to ±28 V, which are easily attained by these types of pickups.

The differential-input 14-pin versions provide the option of setting the input reference level and still having hysteresis around that level to provide excellent noise rejection in any application. The input protection is removed in the 14-pin versions. Therefore, neither of the differential inputs should exceed the limits of the supply voltage. An input must not go below ground without a resistance in the lead to limit the current that will flow in the epi-substrate diode. The charge pump circuit that follows the input stage produces a dc output voltage proportional to the input frequency. The charge pump circuit (see Figure 2) consists of a timing capacitor (C1), an output resistor (R1), and an integrating or filter capacitor (C2). When the input changes state (due to a suitable zero crossing or differential voltage on the input), the timing capacitor is either charged or discharged linearly with a constant current of 200 μA through CAP1 between two voltages whose difference is $V_{CC}/2$. Within one-half cycle of the input frequency or a time equal to 1/2f, the change in charge on C1 is equal to (VCC/2)C1. The average amount of current pumped into or out of the capacitor is:

$$\text{CAP1 current (average)} = \frac{Q}{T} = C1 \cdot \frac{V_{CC}}{2} \cdot 2f = V_{CC} \cdot f \cdot C1$$

The output of the charge pump accurately mirrors the CAP1 current into the load resistor (R1) connected to CPO. If the pulses of current are integrated with a filter capacitor, the output voltage is the average CAP1 current times R1, and the total equation becomes:

$$V_O = V_{CC} \cdot f \cdot C1 \cdot R1 \cdot K$$

where K is the gain factor, which is typically 1.

The size of C2 is dependent only on the amount of ripple allowable and the required response time.

selection of R1, C1, and C2

To achieve optimum performance, there are some limitations to be considered in the selection of R1 and C1. The timing capacitor controls the RC time and provides internal compensation for the charge pump circuit. For very accurate operation it should be 100 pF or greater. Smaller values, especially at lower temperatures, can cause an error current through R1. $V_O/R1$ must be less than or equal to the output current at CPO, which is fixed typically at 180 μA. If R1 is too large it becomes a significant fraction of the output impedance at CPO, which degrades the linearity. In addition, ripple voltage must be considered when selecting R1. The size of C2 is directly affected by the size of R1. An expression that describes the ripple content at CPO is:

$$V_{ripple} = \frac{V_{CC}}{2} \cdot \frac{C1}{C2} \cdot \left(1 - V_{CC} \cdot f \cdot \frac{C1}{200}\right) \quad \text{volts peak-to-peak}$$

where

C1 and C2 are in farads
V_{CC} is in volts
f is in hertz.

TYPICAL APPLICATION DATA

R1 cannot be chosen independently of ripple because response time or the time it takes V_O to stabilize at a new level increases as the size of C2 increases. A compromise between ripple, response time, and linearity must be chosen carefully. As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1, and I_{cap} (current through CAP1).

$$f_{max} = \frac{I_{cap}}{C1 \cdot V_{CC}} \quad \text{hertz}$$

where

I_{cap} is typically 200 μA
C1 is in farads
V_{CC} is in volts.

zener regulator options (LM2917)

For those applications in which an output voltage or current must be obtained independently of supply voltage variations, the LM2917 can be used. The most important factor in selecting a dropping resistor for the unregulated supply is that the frequency-to-voltage converter circuit and the operational amplifier alone require approximately 3 mA at the voltage level set by the zener diode. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the supply voltage varies between 9 and 16 V, a resistance of 470 Ω will minimize the zener voltage variation to typically 160 mV. If the resistance goes under 400 Ω or above 600 Ω, the zener variation quickly rises above 200 mV for the same input variation.

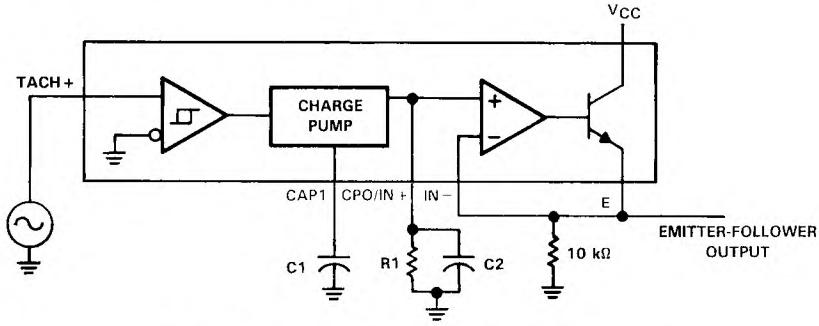

FIGURE 2. MINIMUM-COMPONENT TACHOMETER

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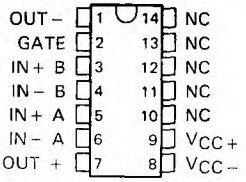
D2572, JANUARY 1980—REVISED APRIL 1988

- Differential Inputs and Outputs
- Channel Select Time . . . 20 ns Typ
- Bandwidth Typically 50 MHz
- 16-dB Minimum Gain
- Common-Mode Rejection Typically 85 dB
- Broadband Noise Typically 25 μV

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

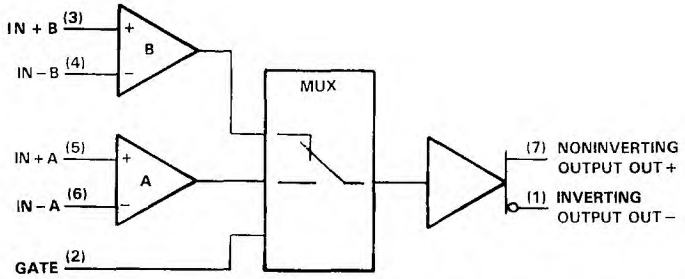
GATE INPUT	SELECT
H	Channel A
L	Channel B

description

The MC1445 is a general-purpose, gated, dual-channel wideband amplifier designed for use in video-signal mixing and switching. Channel selection is accomplished by control of the voltage level at the gate. A high logic level selects channel A; a low logic level selects channel B. The unselected channel will have a gain of one or less.

The MC1445 is characterized for operation from 0°C to 75°C.

block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 12 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±5 V
Output current, I_O . . . . . ±25 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values, except differential input voltage, are with respect to the midpoint of V_{CC+} and V_{CC-}.
2. Differential input voltages are measured at a noninverting input terminal with respect to the appropriate inverting input terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 75°C$ POWER RATING
J	626 mW	8.2 mW/°C	74°C	[illegible] mW
N	625 mW	N/A	N/A	625 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		5	8	V
Supply voltage, V_{CC-}		−5	−8	V
Operating free-air temperature range, T_A	0		75	°C

electrical characteristics at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{VS}	Large-signal single-ended voltage amplification	f = 125 kHz,	V_i = 20 mV	16	19.5	23	dB
BW	Bandwidth	V_i = 20 mV			50		MHz
V_{IO}	Input offset voltage					7.5	mV
I_{IO}	Input offset current				2		μA
I_{IB}	Input bias current				15	30	μA
V_{ICR}	Common-mode voltage range				±2.5		V
V_{OQ}	Quiescent output voltage				0.1		V
ΔV_{OQ}	Change in quiescent output voltage	Gate input change from 5 V to 0 V			±15		mV
V_{OPP}	Maximum peak-to-peak output voltage swing	f = 125 kHz,	R_L = 1 kΩ	1.5	2.5		V
z_i	Input impedance	f = 125 kHz		3	10		kΩ
z_o	Output impedance	f = 50 kHz			25		Ω
CMRR	Common-mode rejection ratio	f = 50 kHz			85		dB
V_n	Broadband equivalent input noise voltage	BW = 5 Hz to 10 MHz, R_S = 50 Ω			25		μV
V_{TH}	High-level gate threshold voltage	$A_{VS(A)} \geq$ 16 dB,	$A_{VS(B)} \leq$ 0 dB		1.3	3	V
V_{TL}	Low-level gate threshold voltage	$A_{VS(B)} \geq$ 16 dB,	$A_{VS(A)} \leq$ 0 dB	0.2	0.4		V
I_{IH}	High-level gate current	V_I = 5 V				4	μA
I_{IL}	Low-level gate current	V_I = 0				4	mA
t_{PLH}	Propagation delay time, low-to-high-level output	ΔV_I = 20 mV,	50% to 50%		6.5		ns
t_{PHL}	Propagation delay time, high-to-low-level output	ΔV_I = 20 mV,	50% to 50%		6.3		ns
t_{TLH}	Transition time, low-to-high-level output	ΔV_I = 20 mV,	10% to 90%		6.5		ns
t_{THL}	Transition time, high-to-low-level output	ΔV_I = 20 mV,	10% to 90%		7		ns
I_{CC+}	Supply current from V_{CC+}	No load,	No signal		7	15	mA
I_{CC-}	Supply current from V_{CC-}	No load,	No signal		−7	−15	mA
P_D	Power dissipation	No load,	No signal		70	150	mW

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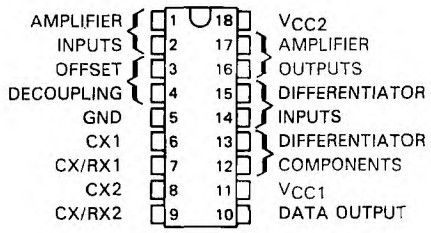
D2759, NOVEMBER 1983—REVISED FEBRUARY 1988

- **Combines All Read-Amplifier Active Circuitry into One Monolithic Circuit**
- **Peak Shift . . . 2% Max (MC3470A)**
- **Designed to be Interchangeable with Motorola MC3470**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)

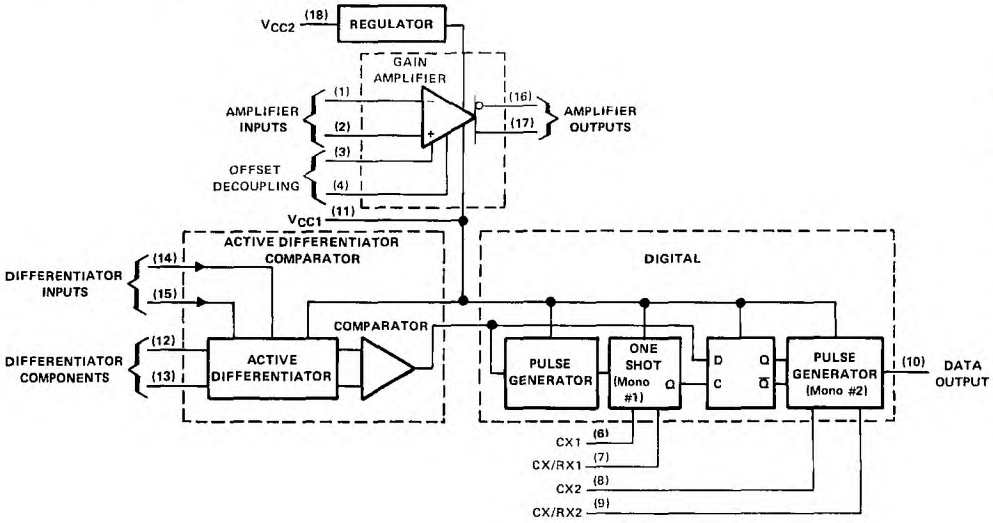


description

The MC3470 and MC3470A are monolithic read-amplifier systems each containing all the active circuitry necessary for obtaining digital information from floppy disk storage. They are designed to accept the ac differential signal from the magnetic head and produce a digital output pulse corresponding to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

The MC3470 and MC3470A are characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 16 V
Input voltage range (amplifier inputs) . . . . . −0.2 V to 7 V
Output voltage, V_O (data output) . . . . . −0.2 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage V_{CC1}		4.75	5	5.25	V
Supply voltage V_{CC2}		10	12	14	V
Timing capacitor CX1 (see Note 2)		[illegible]		[illegible]	pF
Timing capacitor [illegible]		[illegible]		[illegible]	pF
Timing resistors RX1 and RX2		1.5		10	kΩ
Timing of digital section	Monostable no. 1	[illegible]		[illegible]	ns
	Monostable no. 2	[illegible]		[illegible]	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: To minimize current transients, CX1 should be kept as small as convenient.

4 Special Functions

TEXAS INSTRUMENTS
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electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

gain amplifier section

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
A_{VD}	Differential voltage amplification	MC3470	V_{id} = 5 mV rms,	f = 200 kHz	80	100		V/V
		MC3470A			100	110	130	
I_{IB}	Input bias current					−10	−25	μA
V_{ICR}	Common-mode input voltage range		THD ≤ 5%		−0.1 to 1.5			V
V_{IDR}	Differential input voltage range		THD ≤ 5%		±25			mV
V_{OPP}	Peak-to-peak differential output voltage				3	4		V
V_{OC}	Common-mode output voltage		V_I = 0,	V_{ID} = 0		3		V
V_{OD}	Differential output offset voltage		V_I = 0, T_A = 25°C	V_{ID} = 0,			0.4	V
I_{OS}	Short-circuit output current (each amplifier output)		Output shorted to ground			−8		mA
			Output shorted to V_{CC1}		2.8	4		
r_i	Small-signal input resistance		T_A = 25°C		100	250		kΩ
r_o	Small-signal output resistance (single-ended)		V_{CC1} = 5 V, T_A = 25°C	V_{CC2} = 12 V,		15		Ω
BW	Bandwidth (3 dB)		V_{id} = 2 mV rms, V_{CC2} = 12 V,	V_{CC1} = 5 V, T_A = 25°C	5			MHz
CMRR	Common-mode rejection ratio		V_{CC1} = 5 V, A_{VD} = 40 dB, T_A = 25°C	V_{IPP} = 200 mV, f = 100 kHz,	50			dB
k_{SVR}	Supply voltage rejection ratio		A_{VD} = 40 dB, T_A = 25°C	V_{CC1} = 5 ± 0.25 V, V_{CC2} = 12 V	50			dB
				V_{CC1} = 5 V, V_{CC2} = 12 ±2 V	60			
V_n	Equivalent input noise voltage		BW = 10 Hz to 1 MHz, T_A = 25°C			15		μV

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C.

active-differentiator section

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{sink}	Sink current at pins 12 and 13		$V_{OD} = V_{CC1}$		1	1.4		mA
	Peak shift	MC3470	V_{CC1} = 5 V, V_{IDPP} = 1 V, I_{cap} = 500 μA,	V_{CC2} = 12 V, f = 250 kHz, See Figure 1			5%	
		MC3470A					2%	
r_{id}	Differential input resistance					30		kΩ
r_{od}	Differential output resistance					40		Ω

digital section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 10)	V_{CC1} = 4.75 V, I_{OH} = −0.4 mA	V_{CC2} = 12 V,	2.7			V
V_{OL}	Low-level output voltage (pin 10)	V_{CC1} = 4.75 V, I_{OL} = 8 mA	V_{CC2} = 12 V,			0.5	V
I_{CC1}	Supply current from V_{CC1}	V_{CC1} = 5.25 V			35	50	mA
I_{CC2}	Supply current from V_{CC2}	V_{CC2} = 14 V			4.5	10	mA

timing characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_r	Rise time (pin 10)				20	ns
t_f	Fall time (pin 10)				25	ns
	Timing accuracy of monostable no. 1 compared to 0.625 RX1 • CX1 + 200 ns	RX1 = 1.5 kΩ to 10 kΩ, CX1 = 150 pF to 680 pF	85%		115%	
	Timing accuracy of monostable no. 2 compared to 0.625 RX2 • CX2	RX2 = 1.5 kΩ to 10 kΩ, CX2 = 100 pF to 800 pF	85%		115%	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C.

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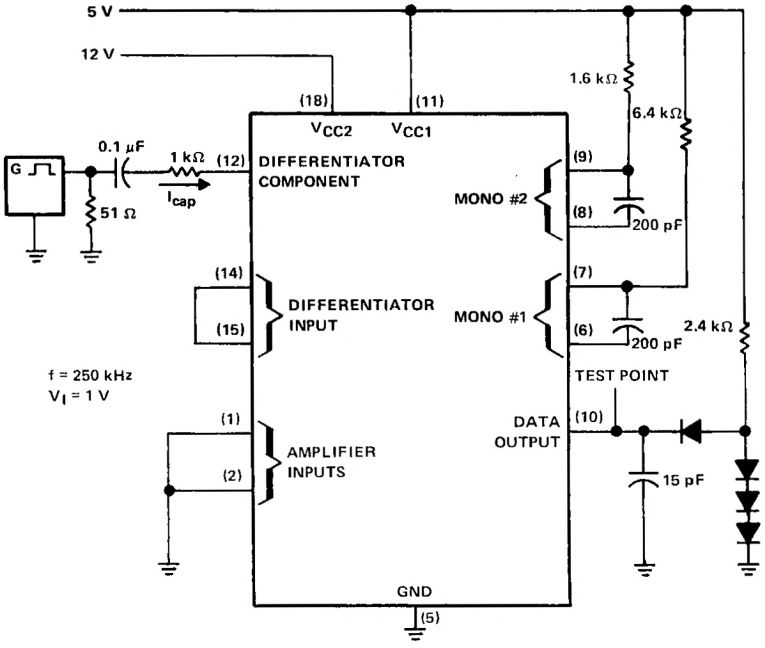
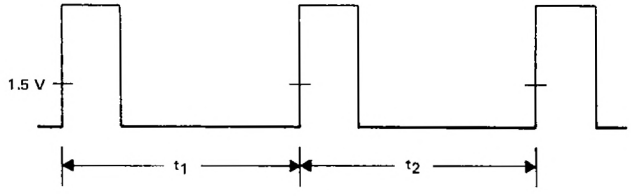
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

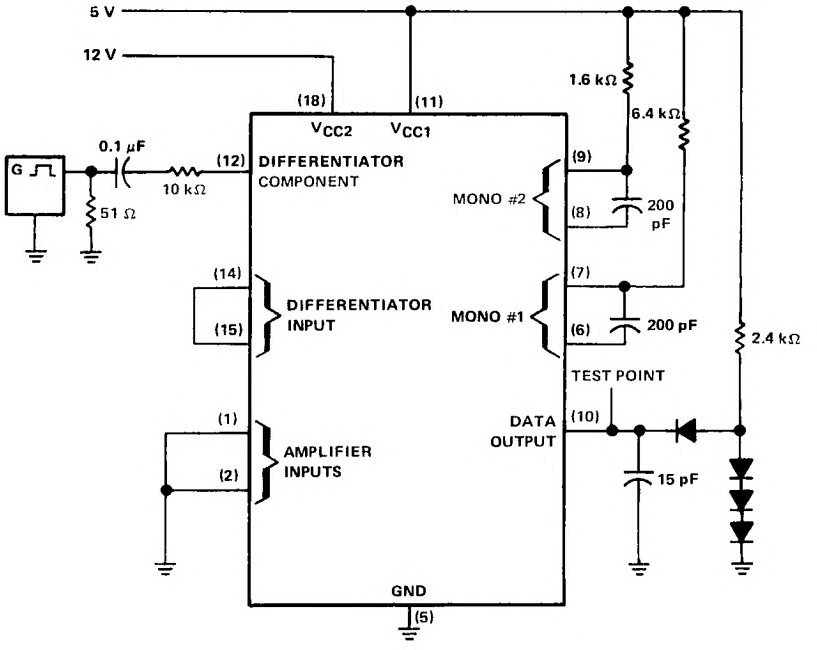


$$\text{Peak shift} = \frac{(t_1 - t_2)}{2\,(t_1 + t_2)} \; 100\%$$

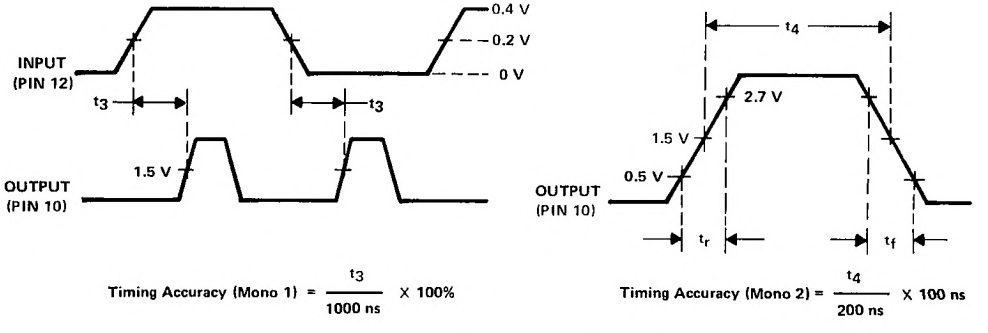
VOLTAGE WAVEFORMS

FIGURE 1. PEAK SHIFT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



$$\text{Timing Accuracy (Mono 1)} = \frac{t_3}{1000\ \text{ns}} \times 100\%$$

$$\text{Timing Accuracy (Mono 2)} = \frac{t_4}{200\ \text{ns}} \times 100\ \text{ns}$$

VOLTAGE WAVEFORMS

FIGURE 2. TIMING ACCURACY

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TYPICAL CHARACTERISTICS

NORMALIZED POWER SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

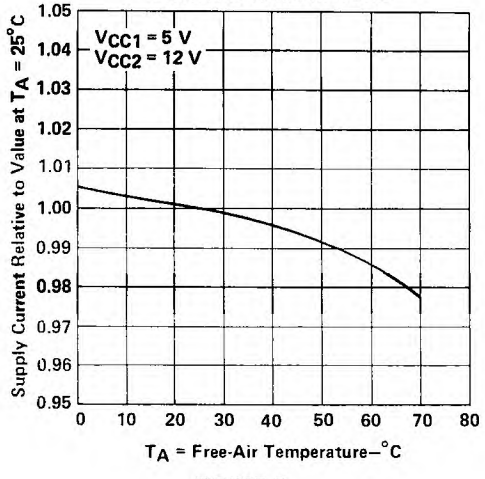

FIGURE 3

NORMALIZED VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

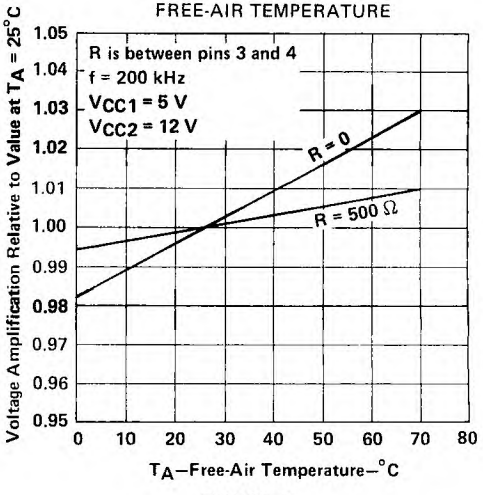

FIGURE 4

NORMALIZED TIME DELAY (PIN 12 TO PIN 10)
vs
FREE-AIR TEMPERATURE

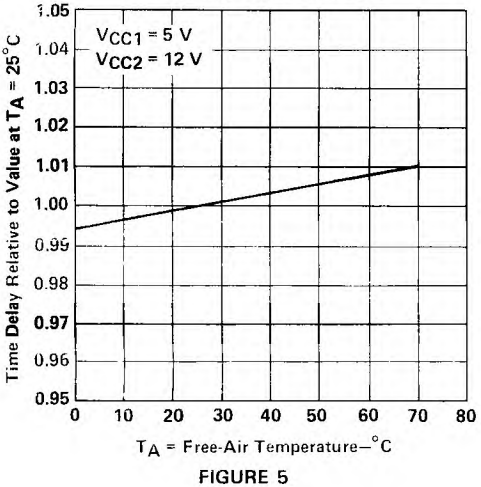

FIGURE 5

VOLTAGE AMPLIFICATION (NORMALIZED)
and PHASE SHIFT
vs
FREQUENCY

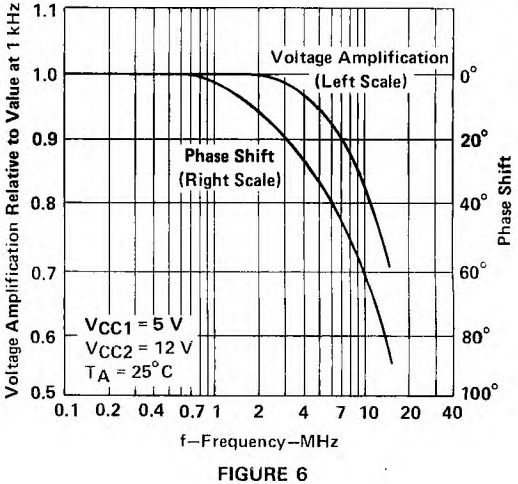

FIGURE 6

TYPICAL APPLICATION INFORMATION

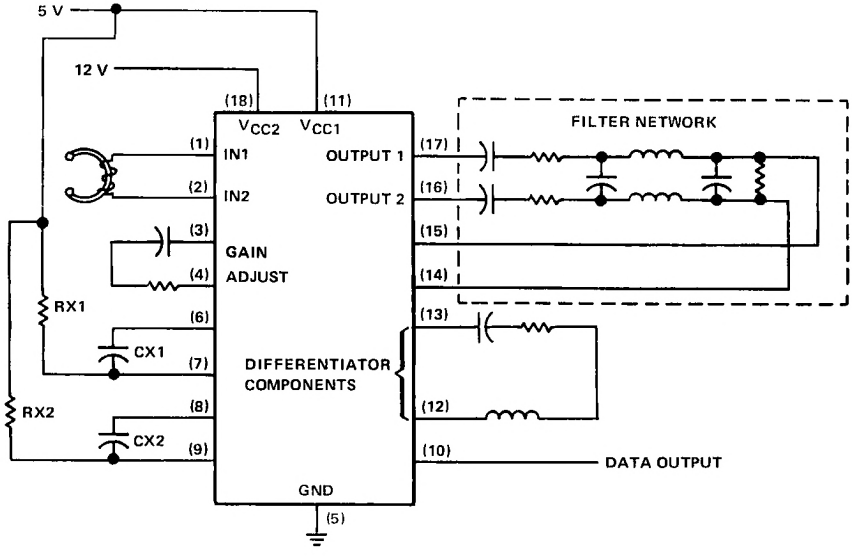

FIGURE 7

TEXAS INSTRUMENTS
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D1669, SEPTEMBER 1973—REVISED OCTOBER 1988

- **Timing from Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source Up to 200 mA**
- **Functionally Interchangeable with the Signetics SE555, SE555C, SA555, NE555; Have Same Pinout**

SE555C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

description

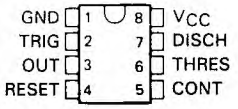
These devices are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

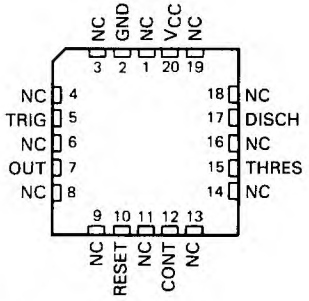
The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The SE555 and SE555C are characterized for operation over the full military range of −55°C to 125°C. The SA555 is characterized for operation from −40°C to 85°C, and the NE555 is characterized for operation from 0°C to 70°C.

SE555, SE555C . . . JG PACKAGE
SA555, NE555 . . . D, JG, OR P PACKAGE
(TOP VIEW)

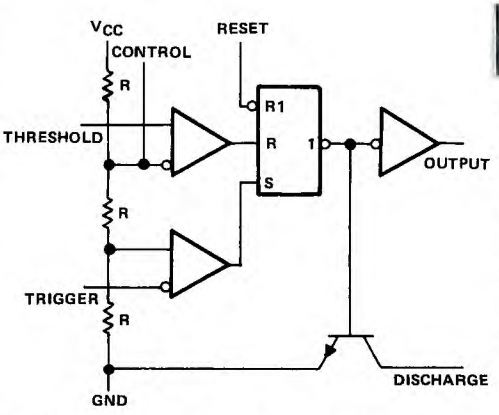


SE555, SE555C . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

functional block diagram



Reset can override Trigger, which can override Threshold.

AVAILABLE OPTIONS

T_A RANGE	V_{thres} MAX V_{CC} = 15 V	PACKAGED DEVICES			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	11.2 V	NE555D		NE555JG	NE555P
−40°C to 85°C	11.2 V	SA555D		SA555JG	SA555P
−55°C to 125°C	10.6 V 11.2 V		SE555FK SE555CFK	SE555JG SE555CJG	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 18 V
Input voltage (control, reset, threshold, and trigger) . . . . . V_{CC}
Output current . . . . . ±225 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range: SE555, SE555C . . . . . −55°C to 125°C
SA555 . . . . . −40°C to 85°C
NE555 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (SE555, SE555C)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (SA555, NE555)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	SE555		SE555C		SA555		NE555		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control, reset, threshold, and trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°C

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electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			SE555C, SA555, NE555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 2)				30	250		30	250	nA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.3	0.7	1	0.3	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1.5	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.2		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is R = R_A + R_B ≈ 3.4 MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE555			SE555C, SA555, NE555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100			100	300	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
§Values specified are for a device in a monostable circuit similar to Figure 9, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
¶Values specified are for a device in an astable circuit similar to Figure 12, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

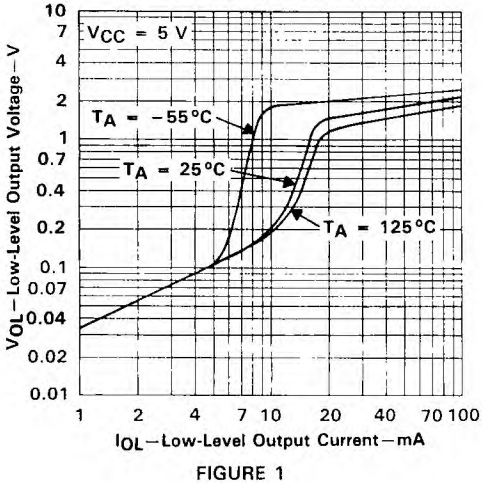

FIGURE 1

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

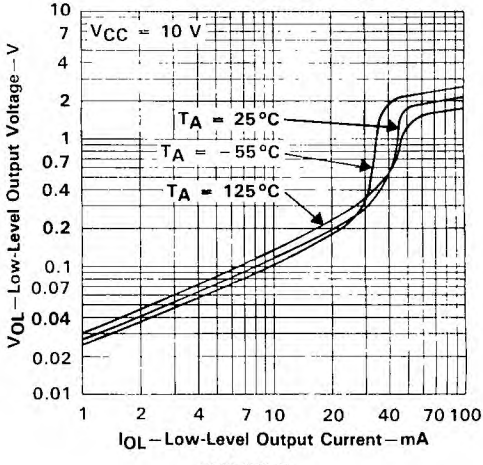

FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

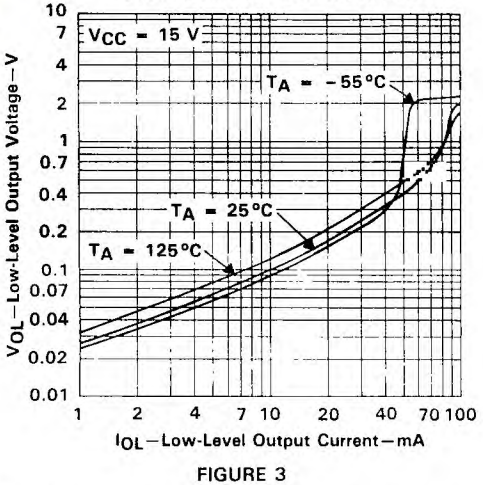

FIGURE 3

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

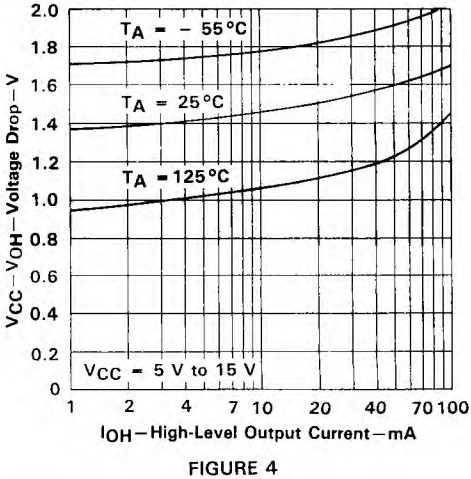

FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

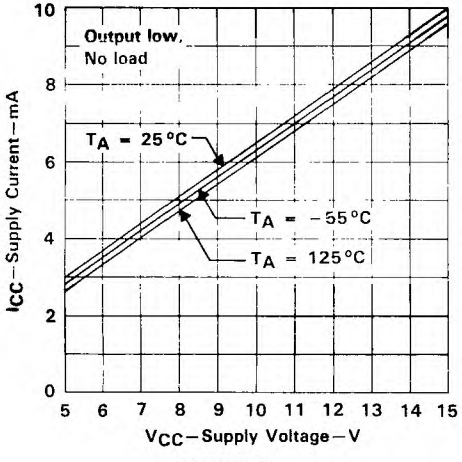

FIGURE 5

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
SUPPLY VOLTAGE

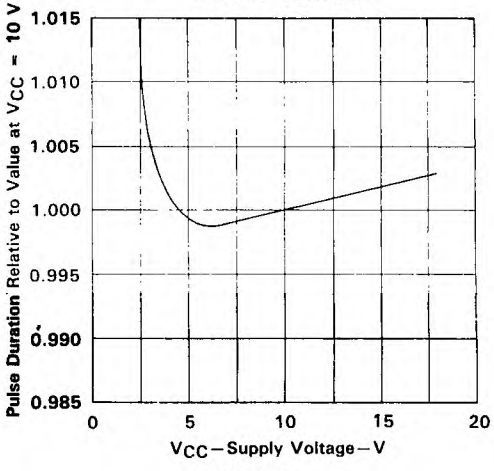

FIGURE 6

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
FREE-AIR TEMPERATURE

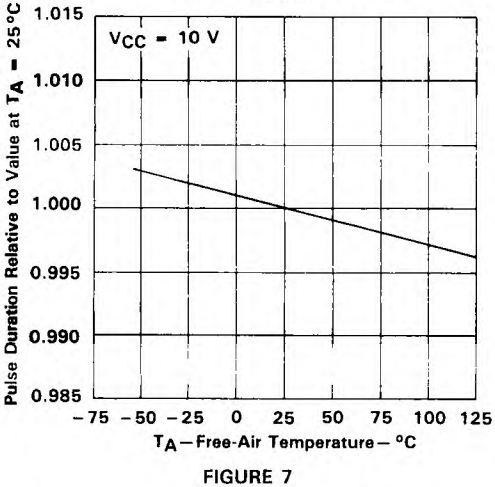

FIGURE 7

PROPAGATION DELAY TIME
vs
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE

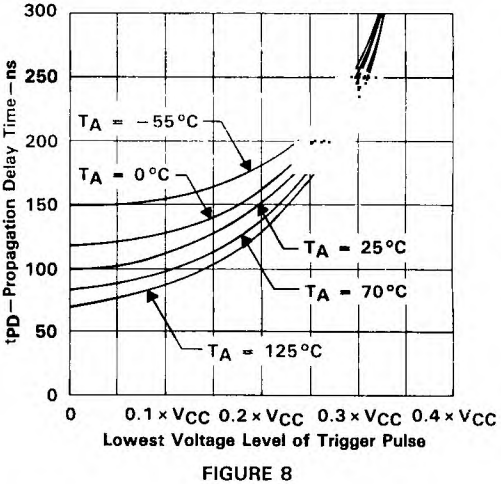

FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

TYPICAL APPLICATION DATA

monostable operation

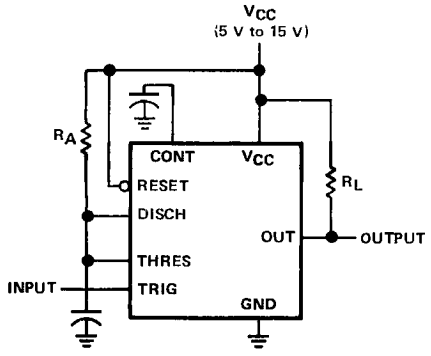

FIGURE 9. CIRCUIT FOR MONOSTABLE OPERATION

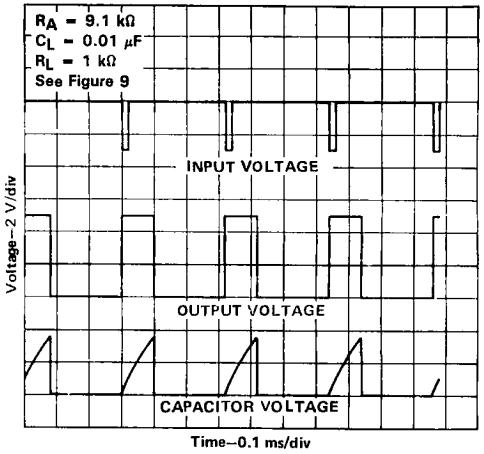

FIGURE 10. TYPICAL MONOSTABLE WAVEFORMS

For monostable operation, any of these timers may be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger input sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold input. If the trigger input has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\overline{Q}$ goes high), drive the output low, and discharge C through Q1.

Monostable operation is initiated when the trigger input voltage falls below the trigger threshold. Once initiated, the sequence ends only if the trigger input is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_W = 1.1\ R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{CC}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to the reset and trigger terminals during the timing interval discharges C and re-initiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when the reset input is not used, it should be connected to V_{CC}.

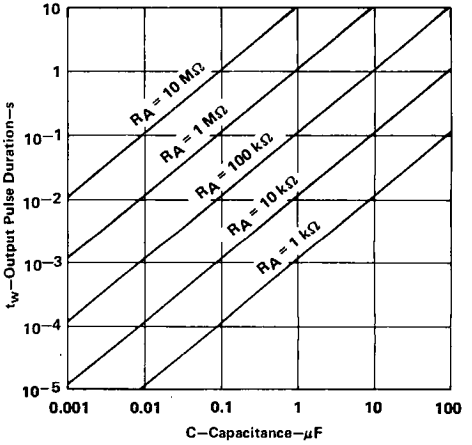

FIGURE 11. OUTPUT PULSE DURATION vs CAPACITANCE

4 Special Functions

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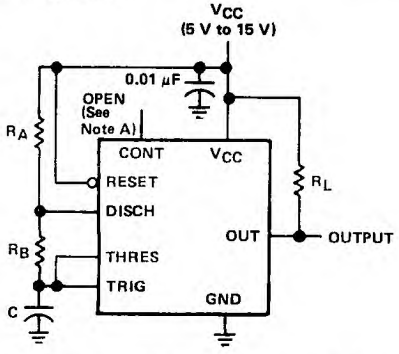
TYPICAL APPLICATION DATA

astable operation



NOTE A: Decoupling the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

FIGURE 12. CIRCUIT FOR ASTABLE OPERATION

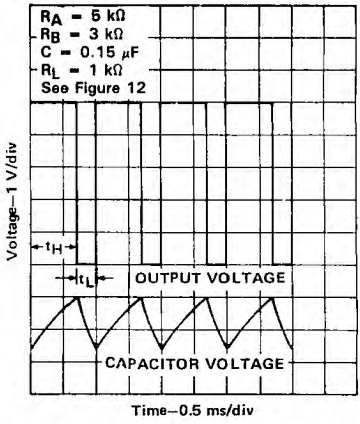


FIGURE 13. TYPICAL ASTABLE WAVEFORMS

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B and then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \cdot V_{CC}$) and the trigger-voltage level ($\approx 0.33 \cdot V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L may be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C$$

$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

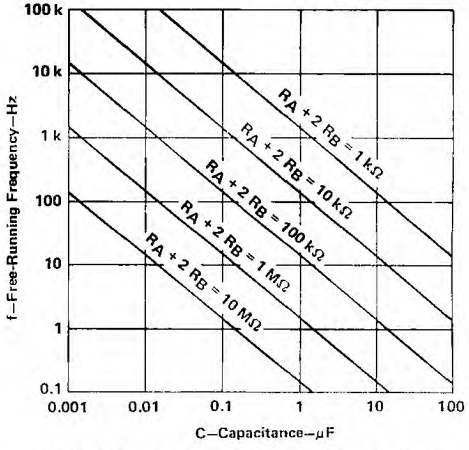


FIGURE 14. FREE-RUNNING FREQUENCY

TYPICAL APPLICATION DATA

missing-pulse detector

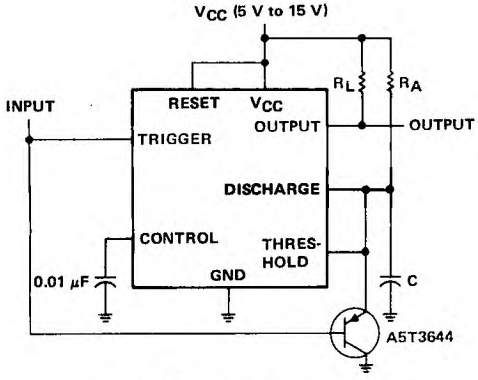


FIGURE 15. CIRCUIT FOR MISSING-PULSE DETECTOR

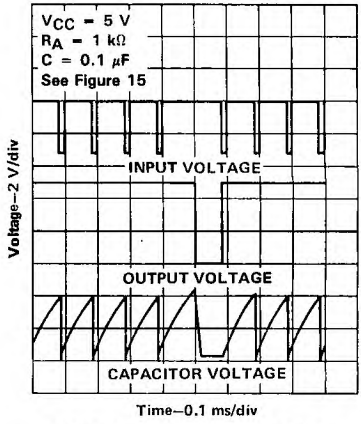


FIGURE 16. MISSING-PULSE DETECTOR WAVEFORMS

The circuit shown in Figure 15 may be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 16.

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 illustrates a divide-by-3 circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

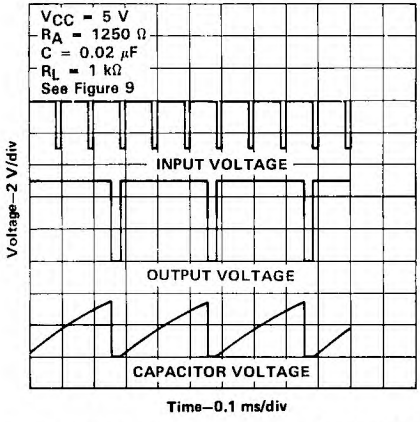


FIGURE 17. DIVIDE-BY-THREE CIRCUIT WAVEFORMS

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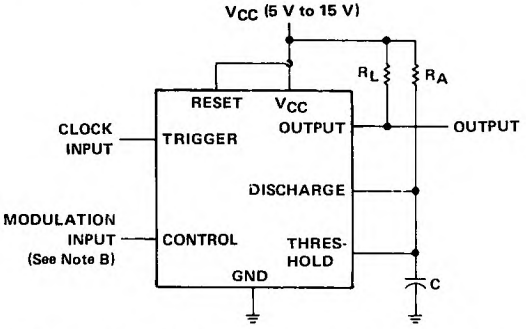
TYPICAL APPLICATION DATA

pulse-width modulation



NOTE B: The modulating signal may be direct or capacitively coupled to the control terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 18. CIRCUIT FOR PULSE-WIDTH MODULATION

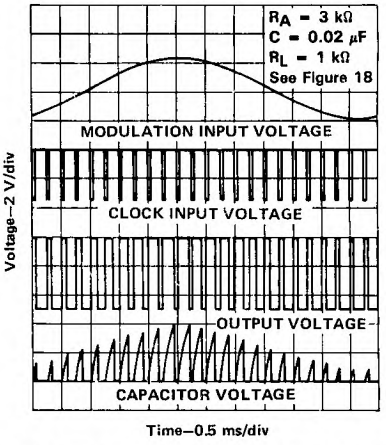
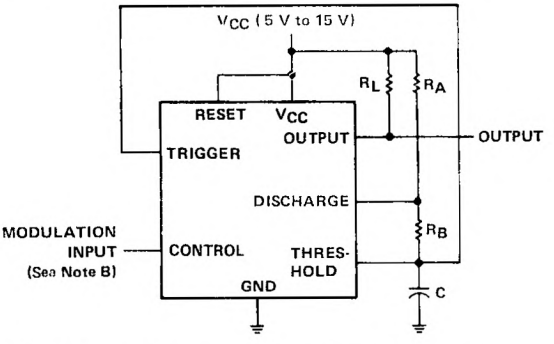


FIGURE 19. PULSE-WIDTH MODULATION WAVEFORMS

The operation of the timer may be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to the control pin. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 illustrates the resulting output pulse-width modulation. While a sine-wave modulation signal is illustrated, any wave shape could be used.

TYPICAL APPLICATION DATA

pulse-position modulation



NOTE B: The modulating signal may be direct or capacitively coupled to the control terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 20. CIRCUIT FOR PULSE-POSITION MODULATION

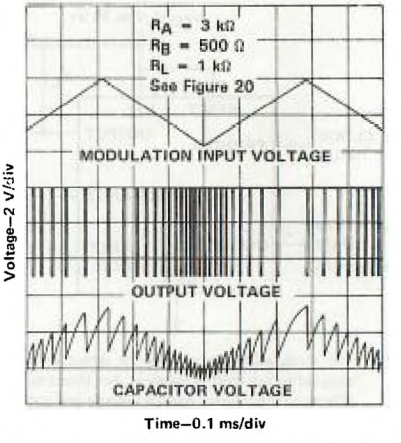


FIGURE 21. PULSE POSITION-MODULATION WAVEFORMS

As shown in Figure 20, any of these timers may be used as a pulse-position modulator. This application modulates the threshold voltage, and thereby the time delay, of a free-running oscillator. Figure 21 illustrates a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

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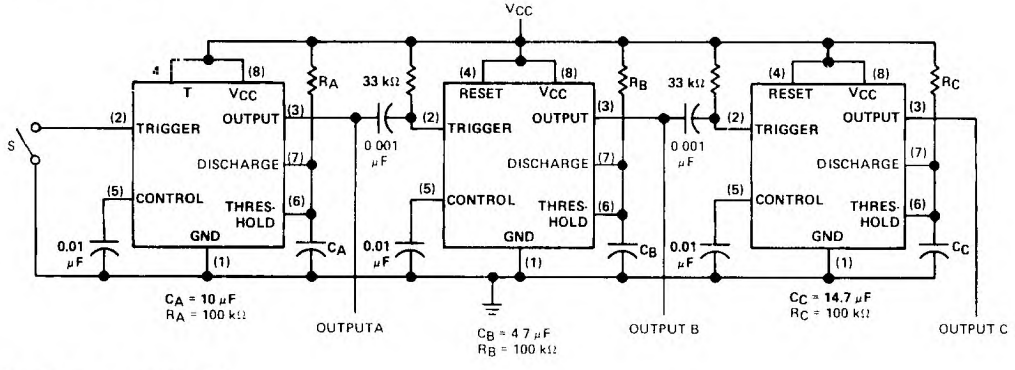
TYPICAL APPLICATION DATA

sequential timer



S closes momentarily at t = 0.

FIGURE 22. SEQUENTIAL TIMER CIRCUIT

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 illustrates a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

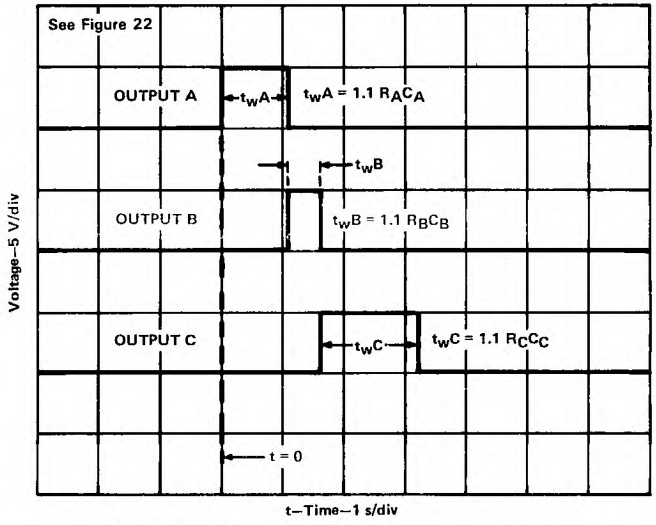


FIGURE 23. SEQUENTIAL TIMER WAVEFORMS

D2440, APRIL 1978—REVISED OCTOBER 1988

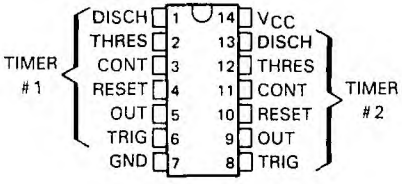
- Two Precision Timing Circuits per Package
- Astable or Monstable Operation
- TTL-Compatible Output Can Sink or Source Up to 150 mA
- Active Pull-Up or Pull-Down
- Designed to be Interchangeable with Signetics SE556, SE556C, SA556, NE556

APPLICATIONS

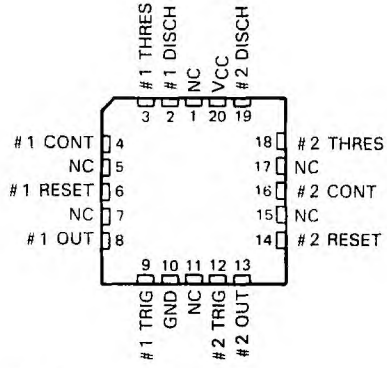
Precision Timer from Microseconds to Hours	Sequential Timer
Pulse-Shaping Circuit	Pulse Generator
Missing-Pulse Detector	Time-Delay Circuit
Tone-Burst Generator	Frequency Divider
Pulse-Width Modulator	Appliance Timer
Pulse-Position Modulator	Industrial Controls
	Touch-Tone Encoder

SE556C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

SE556, SE556C . . . J PACKAGE
SA556, NE556 . . . D, J, OR N PACKAGE
(TOP VIEW)



SE556, SE556C . . . FK PACKAGE
(TOP VIEW)



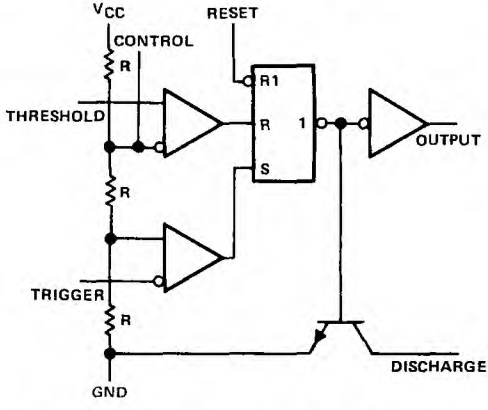
NC—No internal correction

description

These devices provide two monolithic, independent timing circuits of the SE555, SE555C, SA555, or NE555 type in each package. These circuits can be operated in the astable or the monostable mode with external resistor-capacitor timing control. The basic timing provided by the RC time constant may be actively controlled by modulating the bias of the control voltage input.

The threshold and trigger levels are normally two-thirds and one-third respectively of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level,, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

functional block diagram (each timer)



Reset can override Trigger, which can override Threshold.

The SE556 and SE556C are characterized for operation over the full military range of −55°C to 125°C. The SA556 is characterized for operation from −40°C to 85°C, and the NE556 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A RANGE	V_{thres} MAX V_{CC} = 15 V	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	11.2 V	NE556D		NE556J	NE556N
−40°C to 85°C	11.2 V	SA556D		SA556J	SA556N
−55°C to 125°C	10.6 V 11.2 V		SE556FK SE556CFK	SE556J SE556CJ	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE556DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 18 V
Input voltage (control, reset, threshold, and trigger) . . . . . V_{CC}
Output current . . . . . ±225 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range: SE556, SE556C . . . . . −55°C to 125°C
SA556 . . . . . −40°C to 85°C
NE556 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (SE556, SE556C)	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (SA556, NE556)	1025 mW	8.2 mW/°C	656 mW	533 mW	N/A
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	N/A

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recommended operating conditions

	SE556		SE556C		SA556		NE556		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control, reset, threshold, and trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±		±200		±200		±200	mA
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE556			SE556C, SA556, NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 2)				30	250		30	250	nA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.3	0.7	1	0.3	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1.5	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = [illegible] mA		2	2.2		2	2.5	
		I_{OL} = [illegible] mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.15		0.1	0.25	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.3	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = [illegible] mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = [illegible] mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		20	24		20	30	mA
		V_{CC} = 5 V		6	10		6	12	
	Output high, No load	V_{CC} = 15 V		18	20		18	26	
		V_{CC} = 5 V		4	8		4	10	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 1. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4$ MΩ, and for V_{CC} = 15 V, the maximum value is ≈ 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE556			SE556C, SA556, NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
	Timer 1 — Timer 2			±0.5			±1		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
	Timer 1 — Timer 2			±10			±10		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
	Timer 1 — Timer 2			±0.1					
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200			300	ns
Output pulse fall time				100	200		100	300	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
§Values specified are for a device in a monostable circuit similar to Figure 2, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
¶Values specified are for a device in an astable circuit similar to Figure 1, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL APPLICATION DATA

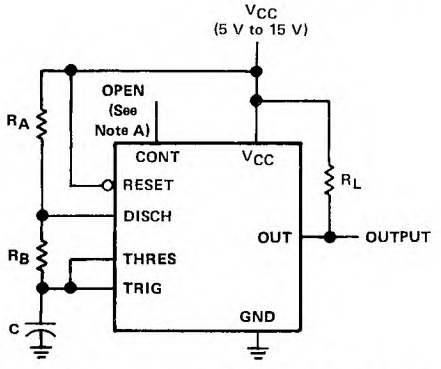

FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

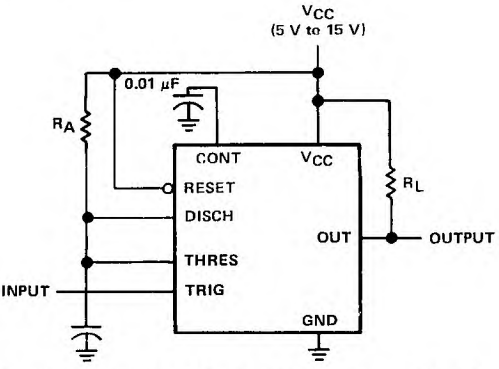

FIGURE 2. CIRCUIT FOR MONOSTABLE OPERATION

NOTE A: Bypassing the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

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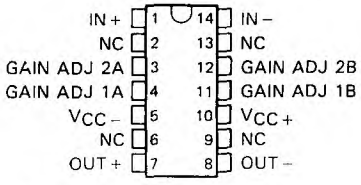
D2667, FEBRUARY 1984—REVISED FEBRUARY 1988

- **90-MHz Bandwidth**
- **Adjustable Gain to 400**
- **No Frequency Compensation Required**
- **Adjustable Passband**
- **Designed to be Interchangeable with Signetics SE592 and NE592**

DEVICE TYPE	TEMPERATURE RANGE	A_{VD} RANGE (GAIN OPTION 1)
SE592	−55°C to 125°C	300—500
NE592	0°C to 70°C	250—600
NE592A	0°C to 70°C	400—600

NE592, NE592A . . . D OR N PACKAGE
SE592 . . . J PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices are monolithic two-stage amplifiers with differential inputs and differential outputs.

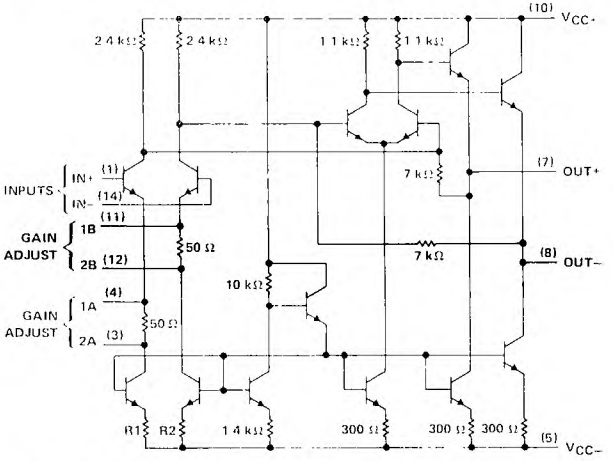
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the devices to drive capacitive loads, and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 100 or 400 may be selected without external components; or amplification may be adjusted from 0 to 400 by the use of a single external resistor connected between the gain-adjustment pins 1A and 1B. External frequency-compensating components are not required for any gain option.

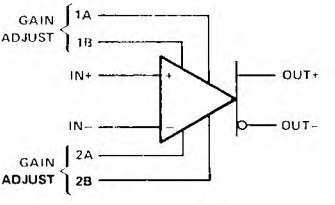
The devices are particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The SE592 is characterized for operation over the full military temperature range of −55°C to 125°C. The NE592 and NE592A are characterized for operation from 0°C to 70°C.

schematic



symbol



All resistor values shown are in ohms and nominal.
In NE592 or SE592, R1 = 500 Ω, R2 = 500 Ω.
In NE592A, R1 = 600 Ω, R2 = 600 Ω.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	8 V
Supply voltage V_{CC-} (see Note 1)	−8 V
Differential input voltage	±5 V
Common-mode input voltage	±6 V
Output current	10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: SE592	−55°C to 125°C
NE592, NE592A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTE 1: All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	N/A	N/A	500 mW	
J	500 mW	11 mW/°C	105°C	500 mW	275 mW
N	500 mW	N/A	N/A	500 mW	

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recommended operating conditions

	SE592			NE592 NE592A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	3	6	8	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	−3	−6	−8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics at 25°C operating free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	SE592 MIN	SE592 TYP	SE592 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	300	400	500	V/V
				2	90	100	110	
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	1		40		MHz
				2		90		
I_{IO}	Input offset current			1, 2, or 3		0.4	3	μA
I_{IB}	Input bias current			1, 2, or 3		9	20	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1, 2, or 3	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{IO} = 0, R_L = ∞	1			1.5	V
				2			1	
				3		0.35	0.75	
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		V
r_i	Input resistance			1		4		kΩ
				2	20	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
kSVR	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5		ns
				2		4.5	10	
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24	mA

†The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	SE592 MIN	SE592 TYP	SE592 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V	1	200		600	V/V
				2	80		120	
I_{IO}	Input offset current			1 or 2			5	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1			1.5	V
				2			1.2	
				3			1	
V_{OPP}	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.5			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	2.5			mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27	mA

†The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B; pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B; pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

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electrical characteristics at 25°C operating free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	NE592			NE592A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	250	400	600	400	440	600	V/V
				2	80	100	120	80	100	120	
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	1		40			40		MHz
				2		90			90		
I_{IO}	Input offset current		V_{IC} = 0	1, 2, or 3		0.4	5		0.4	5	μA
I_{IB}	Input bias current		V_{IC} = 0	1, 2, or 3		9	30		10	30	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞		2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5			1.5	V
				3		0.35	0.75		0.35	0.75	
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		3	4		V
r_i	Input resistance			1		4			4		kΩ
				2	10	30		10	30		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance					2			2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60			60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12			12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5			7.5		ns
				2		6	10		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5			10.5		ns
				2		4.5	12		4.5	12	
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	3	4		3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24		19	24	mA

†The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

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electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	NE592			NE592A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large signal differential voltage amplification	1	V_{OPP} = 3 V	1	250		600	400		600	V/V
				2	80		120	80		120	
I_{IO}	Input offset current			1 or 2			6			6	μA
I_{IB}	Input bias current			1 or 2			40			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5			1.5	V
				3			1			1	
V_{OPP}	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.8			2.8			V
r_i	Input resistance			2	8			8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			50			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3				2.8	4		mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27			27	mA

†The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

PARAMETER MEASUREMENT INFORMATION

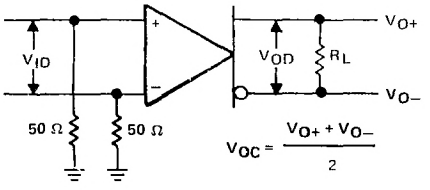


FIGURE 1

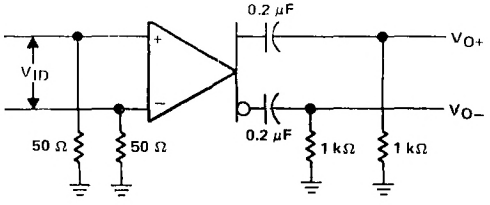


FIGURE 2

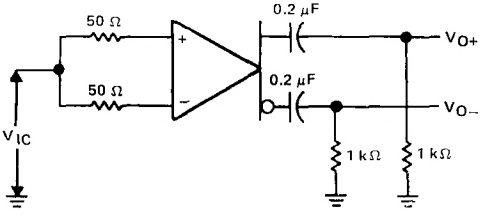


FIGURE 3

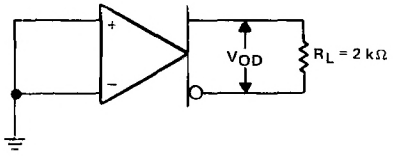
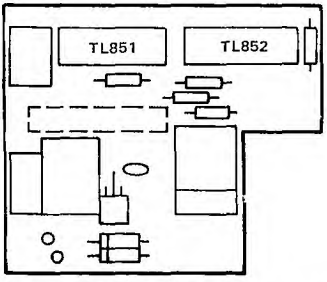


FIGURE 4

D2780, OCTOBER 1983—REVISED MARCH 1988

- **Accurate Sonar Ranging from 6 Inches to 35 Feet**
- **Drives 50-kHz Electrostatic Transducer with No Additional Interface**
- **Operates from Single Supply**
- **Accurate Clock Output Provided for External Use**
- **Selective Echo Exclusion**
- **TTL-Compatible**
- **Multiple Measurement Capability**
- **Uses TL851 and TL852 Sonar Ranging Integrated Circuits**



See schematic, Figure 4, for terminal assignments.

description

The SN28827 is an economical sonar ranging module that can drive a 50-kHz, 300-V electrostatic transducer with no additional interface. This module, with a simple interface, is able to measure distances of from 6 inches to 35 feet. The typical absolute accuracy is ±2% at one foot or greater.

This module has an external blanking input that allows selective echo exclusion for operation in a multiple-echo mode. The module is able to differentiate echos from objects that are only three inches apart. The digitally controlled-gain, variable-bandwidth amplifier minimizes noise and sidelobe detection in sonar applications.

The module has an accurate ceramic-resonator-controlled 420-kHz time-base generator. An output based on the 420-kHz time base is provided for external use. The sonar transmit output is 16 pulses at a frequency of 49.4 kHz.

The SN28827 operates over a supply voltage range of from 4.5 V to 6.8 V and is characterized for operation from 0°C to 40°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage from any pin to ground (see Note 1)	7 V
Voltage from any pin except XDCR to V_{CC} (see Note 1)	−7 V to 0.5 V
Operating free-air temperature range	0°C to 40°C
Storage temperature range	−40°C to 85°C

NOTE 1: The XDCR pin may be driven from −1 V to 300 V typical with respect to ground.

recommended operating conditions

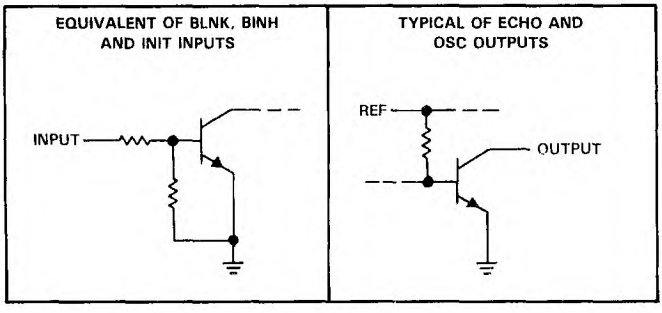
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK,	2.1		V
Low-level input voltage, V_{IL}	BLNK,		0.6	V
ECHO and OSC output			6.8	V
Delay time, power up to	high	5		ms
Recycle period		80		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	OSC	V_{OH} = 5.5 V			100	μA
Low-level output voltage, V_{OL}	ECHO, OSC	I_{OL} = 1.6 mA			0.4	V
Transducer bias voltage						V
Transducer output v	peak-to-peak)					V
Number of cycles fo	output to reach 300 V	C = 500 pF			7	
Internal blanking interval		See Note 2		2.38		ms
Frequency during 16-pulse transmit period	output	See Note 2		49.4		kHz
	output			49.4		
Frequency after 16-pulse transmit period	OSC output	See Note 2		93.3		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				2000	mA
	After transmit period				100	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 2: These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operation with Polaroid electrostatic transducer

There are two basic modes of operation for the SN28827 Sonar ranging module: single-echo mode and multiple-echo mode. The application of power (V_{CC}), the activation of the Initiate (INIT) input, and the resulting transmit output, and the use of the Blanking Inhibit (BINH) input are basically the same for either mode of operation. After applying power (V_{CC}), a minimum of 5 ms must elapse before the INIT input can be taken high. During this time, all internal circuitry is reset and the internal oscillator stabilizes. When INIT is taken high, drive to the Transducer (XDCR) output occurs. Sixteen pulses at 49.4 kHz with 300-V amplitude will excite the transducer as transmission occurs. At the end of the 16 transmit pulses, a dc bias of 150 V will remain on the transducer as recommended for optimum operation by the transducer manufacturer.

In order to eliminate ringing of the transducer from being detected as a return signal, the receive (REC) input of the ranging control IC is inhibited by internal blanking for 2.38 ms after the initiate signal. If a reduced blanking time is desired, then the BINH input can be taken high to end the blanking of the Receive input anytime prior to internal blanking. This may be desired to detect objects closer than 1.33 feet corresponding to 2.38 ms and may be done if transducer damping is sufficient that ringing is not detected as a return signal.

In the single-echo mode of operation (Figure 1), all that must be done next is to wait for the return of the transmitted signal, traveling at approximately 0.9 ms per foot out and back. The returning signal is amplified and appears as a high-logic-level echo output. The time between INIT going high and the echo (ECHO) output going high is proportional to the distance of the target from the transducer. If desired, the cycle can now be repeated by returning INIT to a low-logic level and then taking it high when the next transmission is desired.

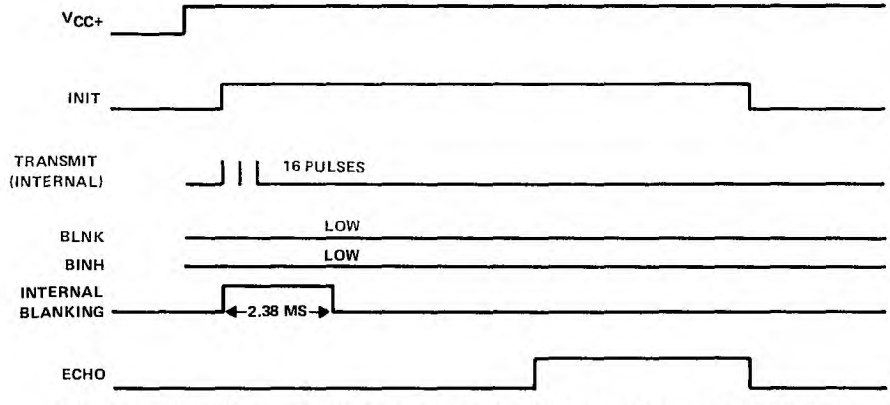


FIGURE 1. EXAMPLE OF A SINGLE-ECHO-MODE CYCLE WITHOUT BLANKING INPUT

If there is more than one target and multiple echos are to be detected from a single transmission, then the cycle is slightly different (Figure 2). After receiving the first return signal, which causes the ECHO output to go high, the Blanking (BLNK) input must be taken high then back low to reset the Echo output for the next return signal. The blanking signal must be at least 0.44 ms in duration to account for all 16 returning pulses from the first target and allow for internal delay times. This corresponds to the two targets being 3 inches apart.

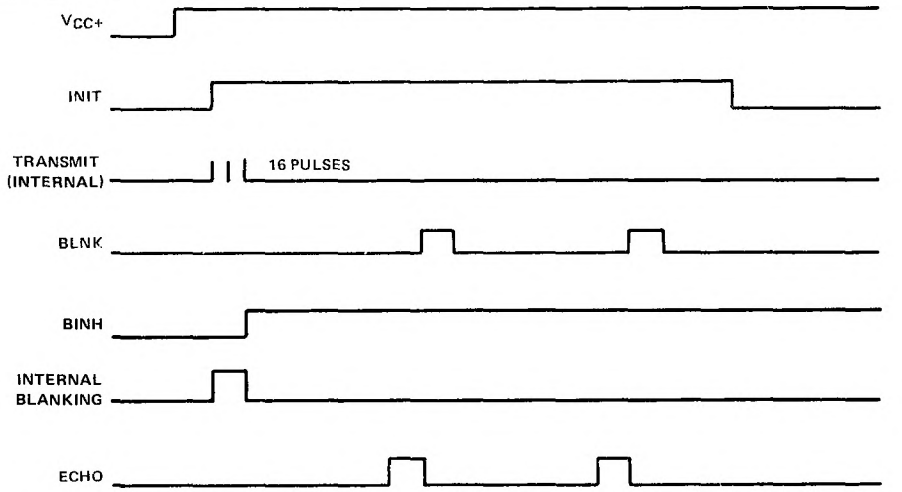


FIGURE 2. EXAMPLE OF A MULTIPLE-ECHO-MODE CYCLE WITH BLANKING INPUT

During a cycle starting with INIT going high, the receiver amplifier gain is incremented higher at discrete times (Figure 3) since the transmitted signal is attentuated with distance. At approximately 38 ms, the maximum gain is attained. For this reason, sufficient gain may not be available for objects greater than

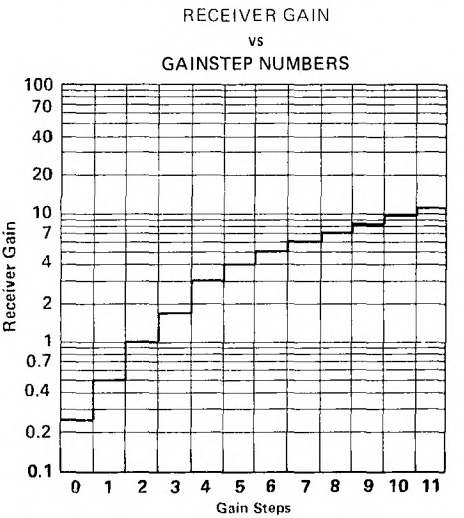


FIGURE 3

TEXAS INSTRUMENTS
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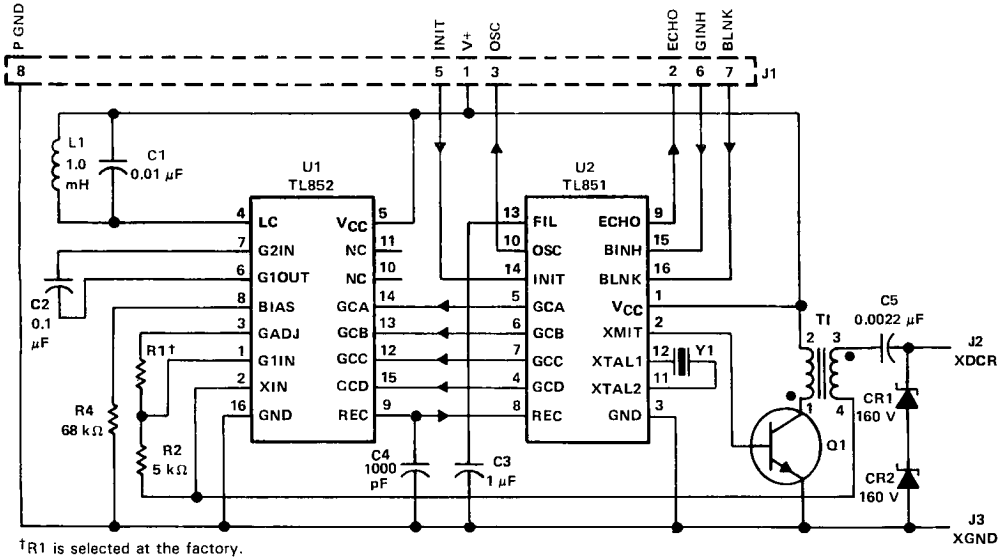
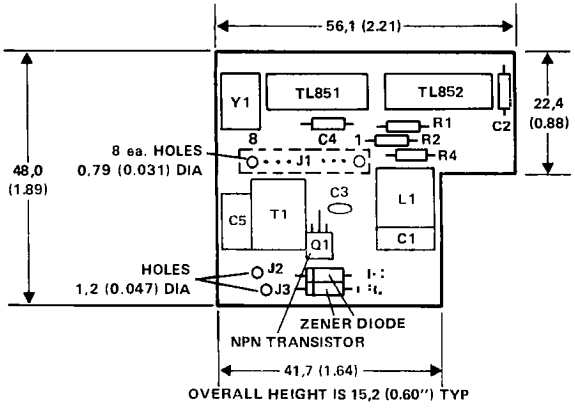
35 feet away. Although gain can be increased by varying R1 (Figure 4), there is a limit to which the gain can be increased for reliable module operation. This will vary from application to application. The modules are "kitted" prior to their final test during manufacture. This is necessary because the desired gain distribution is much narrower than the module gain distribution if all were kitted with one value resistor. As kitted, these modules will perform satisfactorily in most applications. As a rule of thumb, the gain can be increased by up to a factor of 4, if required, by increasing R1 correspondingly. Gain is directly proportional to R1.



†R1 is selected at the factory.

FIGURE 4. SCHEMATIC

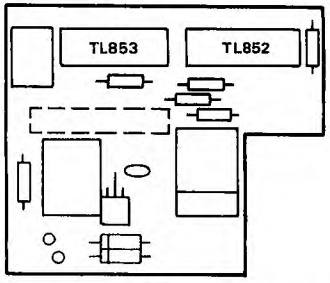


NOTE All dimensions are in millimeters and parenthetically in inches.

FIGURE 5. COMPONENT LAYOUT AND DIMENSIONS OF MODULE

D2842, JANUARY 1985

- **Accurate Sonar Ranging from 6 Inches to 35 Feet**
- **Drives 40-kHz Piezoelectric Transducer**
- **Operates from Single Supply**
- **Accurate Clock Output Provided for External Use**
- **Selective Echo Exclusion**
- TTL-Compatible
- **Multiple Measurement Capability**
- **Uses TL852 and TL853 Sonar Ranging Integrated Circuits**



See schematic, Figure 4, for terminal assignments.

description

The SN28828 is an economical sonar ranging module that can drive a 40-kHz piezoelectric transducer with no additional interface. This module, with a simple interface, is able to measure distances ranging from 6 inches to 35 feet. The typical absolute accuracy is ±2% at one foot or greater.

This module has an external blanking input that allows selective echo exclusion for operation in a multiple-echo mode. The module is able to differentiate echos from objects that are only 3.5 inches apart. The digitally controlled-gain, variable-bandwidth amplifier minimizes noise and side-lobe detection in sonar applications.

The module has an accurate ceramic-resonator-controlled 420-kHz time-base generator. An output based on the 420-kHz time base is provided for external use. The sonar transmit output is 16 pulses at a frequency of 40 kHz.

The SN28828 operates over a supply voltage range of from 4.5 V to 6.8 V and is characterized for operation from 0°C to 40°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage from any pin to ground (see Note 1)	7 V
Voltage from any pin except XDCR to V_{CC} (see Note 1)	−7 V to 0.5 V
Operating free-air temperature range	0°C to 40°C
Storage temperature range	−40°C to 85°C

NOTE 1: The XDCR pin may be driven to ±35 V typical with respect to ground.

recommended operating conditions

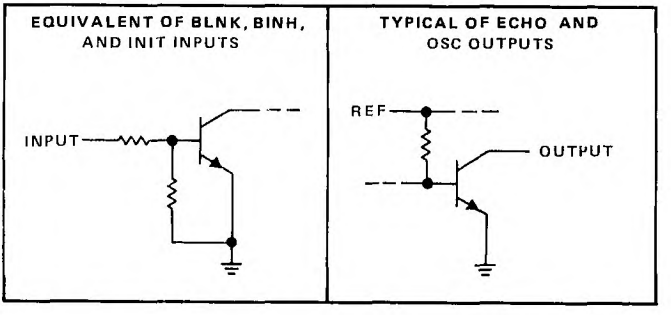
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
· ·level · ·voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
· ·O and ·output voltage			6.8	V
Delay time, power up to INIT high		5		ms
Recycle period		80		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	E	V_{OH} = 5.5 V				µA
Low-level output voltage, V_{OL}	E	I_{OL} = 1.6 mA			0.4	V
Transducer output voltage (peak-to-peak)				70		V
Internal blanking interval		See Note 2		2.46		ms
Frequency during 16-pulse transmit period	OSC output	See Note 2		40		kHz
	·output			40		
Frequency after 16-pulse transmit period	·output	See Note 2		93.3		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				350	mA
	After transmit period				100	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 2: These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



TEXAS INSTRUMENTS
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operation with 40-kHz piezoelectric transducer

There are two basic modes of operation for the SN28828 Sonar ranging module: single-echo mode and multiple-echo mode. The application of power (V_{CC}), the activation of the Initiate (INIT) input and the resulting transmit output, and the use of the Blanking Inhibit (BINH) input are basically the same for either mode of operation. After applying power (V_{CC}), a minimum of 5 ms must elapse before the INIT input can be taken high. During this time, all internal circuitry is reset and the internal oscillator stabilizes. When INIT is taken high, drive to the Transducer (XDCR) output occurs. Sixteen pulses at 40 kHz with 70-V peak-to-peak amplitude will excite the transducer as transmission occurs.

In order to eliminate ringing of the transducer from being detected as a return signal, the Receive (REC) input of the ranging control IC is inhibited by internal blanking for 2.46 ms after the initiate signal. If a reduced blanking time is desired, then the BINH input can be taken high to end the blanking of the Receive input anytime prior to internal blanking. This may be desired to detect objects closer than 1.37 feet corresponding to 2.46 ms and may be done if transducer damping is sufficient that ringing is not detected as a return signal.

In the single-echo mode of operation (Figure 1), all that must be done next is to wait for the return of the transmitted signal, traveling at approximately 0.9 ms per foot out and back. The returning signal is amplified and appears as a high-logic-level echo output. The time between INIT going high and the Echo (ECHO) output going high is proportional to the distance of the target from the transducer. If desired, the cycle can now be repeated by returning INIT to a low-logic level and then taking it high when the next transmission is desired.

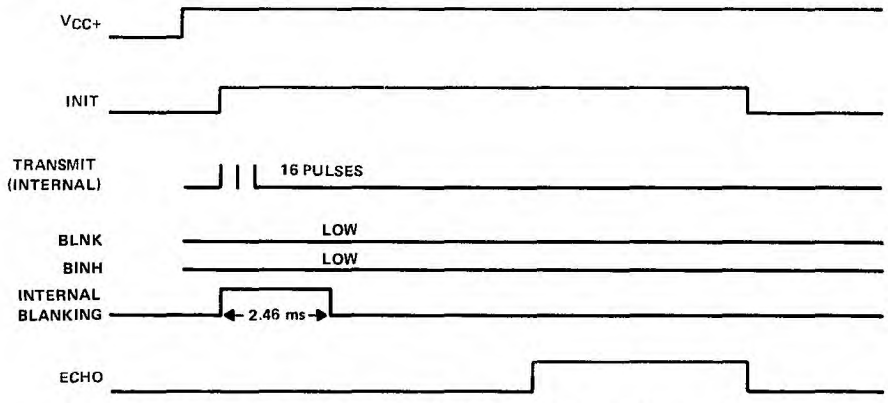

FIGURE 1. EXAMPLE OF A SINGLE-ECHO-MODE CYCLE WITHOUT BLANKING INPUT

If there is more than one target, and multiple echos are to be detected from a single transmission, then the cycle is slightly different (Figure 2). After receiving the first return signal, which causes the ECHO output to go high, the Blanking (BLNK) input must be taken high then back low to reset the Echo output for the next return signal. The blanking signal must be at least 0.52 ms in duration to account for all 16 returning pulses from the first target and allow for internal delay times. This corresponds to the two targets being 3.5 inches apart.

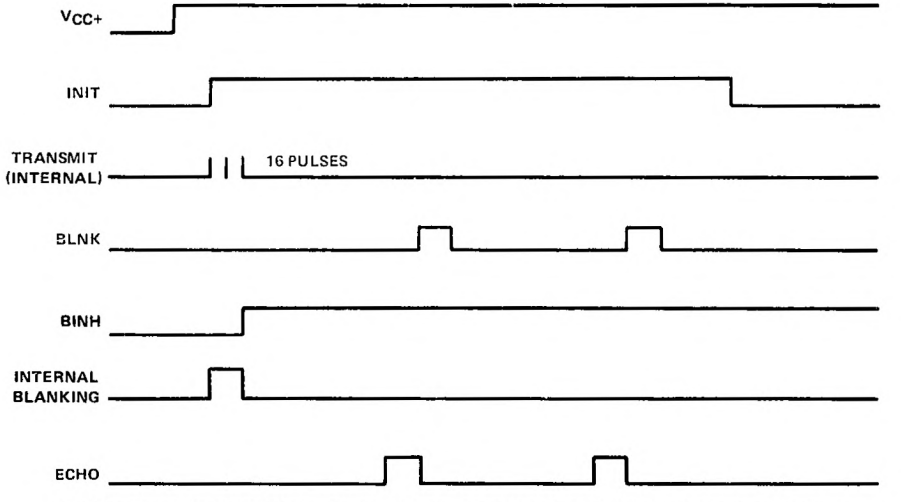

FIGURE 2. EXAMPLE OF A MULTIPLE-ECHO-MODE CYCLE WITH BLANKING INPUT

During a cycle starting with INIT going high, the receiver amplifier gain is incremented higher at discrete times (Figure 3) since the transmitted signal is attenuated with distance. At approximately 38 ms, the maximum gain is attained. For this reason, sufficient gain may not be available for objects greater than

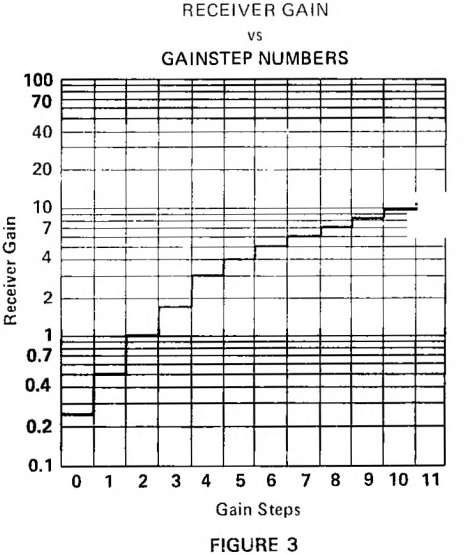

FIGURE 3

TEXAS INSTRUMENTS
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35 feet away. Although gain can be increased by varying R1 (Figure 4), there is a limit to which the *gain* can be increased for reliable module operation. This will vary from application to application. The modules are "kitted" prior to their final test during manufacture. This is necessary because the desired gain distribution is much narrower than the module gain distribution if all were kitted with one value resistor. As kitted, these modules will perform satisfactorily in most applications. As a rule of thumb, the gain can be increased by up to a factor of 3, if required, by increasing R1 correspondingly. Gain is directly proportional to R1.

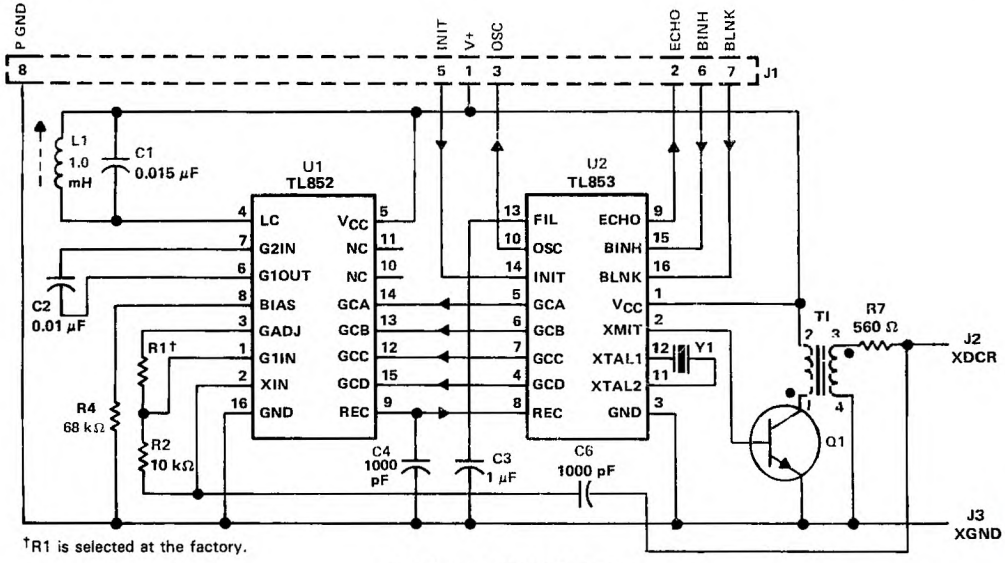
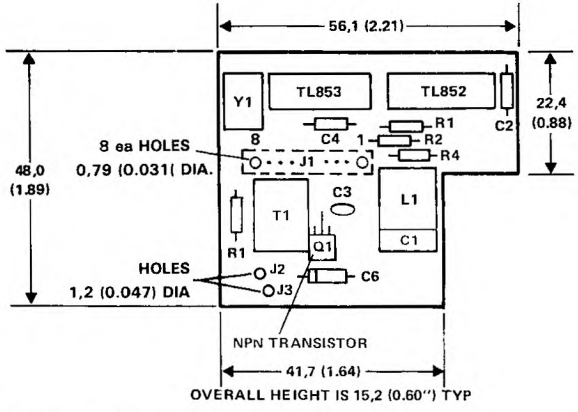


FIGURE 4. SCHEMATIC



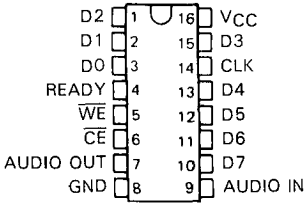
NOTE: All dimensions are in millimeters and parenthetically in inches.

FIGURE 5. COMPONENT LAYOUT AND DIMENSIONS OF MODULE

D2801, JUNE 1984 – REVISED JANUARY 1989

- Each Circuit Contains 3 Programmable Tone Generators
- Programmable White-Noise Generator
- Programmable Attenuation
- Simultaneous Sounds
- Up to 500 kHz Clock Input for SN76494 and 4 MHz for SN76496
- External Audio Input for SN76496 May Be Summed with Internally Generated Tones
- The SN76494A and SN76496A are Interchangeable with the SN76494 and SN76496, Respectively

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

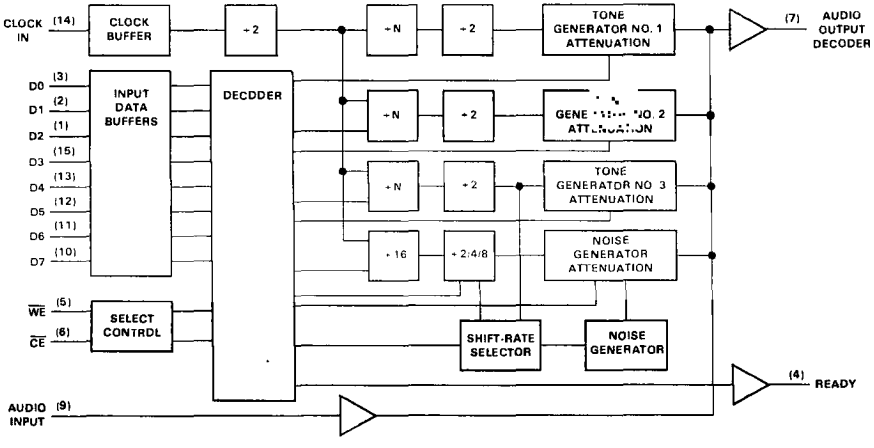
The SN76494 and SN76494A digital complex sound generators are integrated injection logic (I^2L) tone generators designed to provide low-cost tone or noise generation capability in microprocessor systems. The SN76494 and SN76494A are data-bus-based input-output peripheral devices that interface the microprocessor through 8 data lines and 3 control lines.

The SN76494 and SN76494A are identical to the SN76496 and SN76496A except that the maximum clock input frequency for SN76494 and SN76494A is 500 kHz and for SN76496 and SN76496A, it is 4 MHz. A "divide-by-eight" stage is deleted from the SN76496 and SN76496A circuitry so that only 4 clock pulses are required to load the data into the SN76494 and SN76494A, compared to 32 pulses for the SN76496 and SN76496A.

Either of these devices may also be used as a replacement for the SN76489A in all applications if pin 9 is left open or grounded. The output load must be limited to 10 mA.

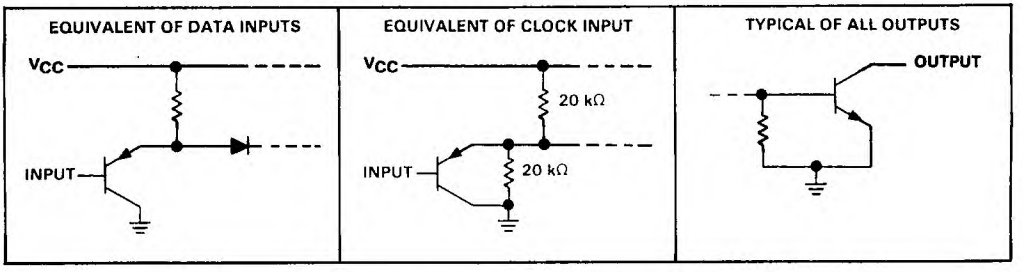
When audio input is not desired in the SN76494, SN76494A, SN76496 or SN76496A, the audio input pin should be grounded.

functional block diagram



4 Special Functions

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: Audio input . . . . . 0.9 V
All other inputs . . . . . 7 V
Output current at pin 7 . . . . . 10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		SN76494, SN76494A			SN76496, SN76496A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_I	Audio input current	0		1.8	0		1.8	mA
V_{OH}	High-level output voltage (pin 4)			5.5			5.5	V
I_{OL}	Low-level output current (pin 4)			2			2	mA
f_{clock}	Input clock frequency			0.5			4	MHz
$t_{d(WE)}$	Delay time, $\overline{CE}$ low to $\overline{WE}$ low	0			0			ns
t_{su}	Setup time, data before $\overline{WE}\downarrow$ or $\overline{CE}\downarrow$	0			0			ns
t_h	Hold time, data after READY↑	0			0			ns
T_A	Operating free-air temperature	0		70	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current (pin 4)		V_O = 5.5 V			10	µA
I_{IH}	High-level input current (All digital inputs)		$V_I = V_{CC}$			10	µA
I_{IL}	Low-level input current	$\overline{CE}$ input	V_I = 0		−25	−175	µA
		All other digital inputs			−10	−70	
V_{IB}	Input bias voltage, audio (pin 9)		R = 4.7 kΩ to V_{CC}	0.5	0.7	0.9	V
V_{OH}	High-level output voltage (pin 7)					5.5	V
V_{OL}	Low-level output voltage (pin 4)		I_{OL} = 2 mA		0.25	0.4	V
V_{OPP}	Peak-to-peak output voltage (pin 7)		V_{CC} = 5 V, Attenuation: Generator under test = 0 dB, All other generators = 30 dB	260			mV
I_{CC}	Supply current				30	50	mA
	Attenuation	2 dB NOM	See Table 1	1	2	3	dB
		4 dB NOM		3	4	5	
		8 dB NOM		7	8	9	
		16 dB NOM		15	16	17	
C_i	Input capacitance					15	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level RDY output from $\overline{CE}$	C_L = 225 pF, R_L = 2 kΩ to V_{CC}		90	150	ns
t_{PHL}	Propagation delay time high-to-low level, RDY output from $\overline{WE}$			90		ns
t_{PLH}	Propagation delay time low-to-high level, RDY output from CLK			90		ns

PARAMETER MEASUREMENT INFORMATION

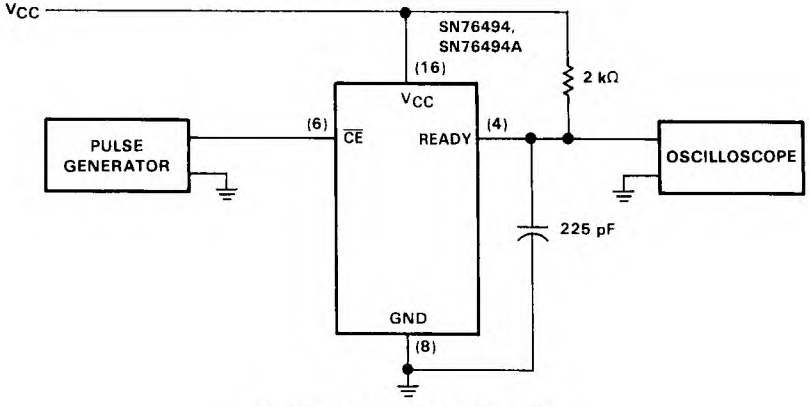


FIGURE 1. t_{PHL} TEST CIRCUIT

pin assignments and functions

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{CE}$	6	I	Chip Enable. When chip enable is low, the device is operational, input terminals are enabled, and data may be entered.
D0 (MSB)	3	I	D0 through D7 – Input data bus
D1	2	I	
D2	1	I	
D3	15	I	
D4	13	I	
D5	12	I	
D6	11	I	
D7 (LSB)	10	I	
V_{CC}	16	I	Supply voltage (5 V nom)
GND	8	O	Ground reference
CLOCK	14	I	Input Clock
$\overline{WE}$	5	I	Write Enable. When $\overline{CE}$ is enabled and $\overline{WE}$ is active (low), input on the data bus is accepted. $\overline{CE}$ and $\overline{WE}$ must be held low until READY returns high (four clock cycles for the SN76494 and SN76494A or 32 clock cycles for the SN76496 and SN76496A). If $\overline{WE}$ remains low throughout four additional clock cycles for the SN76494 and SN76494A (32 clock cycles for the SN76496 and SN76496A) a new write cycle will be initiated.
READY	4	O	When low, READY indicates that a write cycle is in progress; data on the input bus must remain valid until READY returns high.
AUDIO IN	9	I	Audio input from external source
AUDIO OUT	7	O	Audio Drive Out

PRINCIPLES OF OPERATION

tone generators

Each tone generator consists of a frequency synthesis section and an attenuation section. The frequency synthesis section requires 10 bits of information (F0-F9) to define half the period of the desired frequency (f). F0 is the most significant bit and F9 is the least significant bit. This information is loaded into a 10-stage tone counter, which counts down at an N/2 rate where N is the input clock frequency. When the tone counter counts down to zero, a borrow signal is produced. This borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.

The frequency can be calculated by the following:

$$f = \frac{N}{4n} \text{ for SN76494 and SN76494A, or } f = \frac{N}{32n} \text{ for SN76496 and SN76496A}$$

where N = clock in Hz
n = 10-bit binary number

The output level of each tone/noise generator may be selected by programming a four stage attenuator. The attenuator values, along with their bit position in the data word, are shown in Table 1. Multiple attenuation control bits may be true simultaneously. Thus, the maximum attenuation is 30 dB.

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TABLE 1. ATTENUATION CONTROL

BIT POSITION				WEIGHT
A0	A1	A2	A3	(In dB)
0	0	0	1	2
0	0	1	0	4
0	1	0	0	8
1	0	0	0	16
1	1	1	1	OFF

noise generator

The noise generator consists of a noise source and an attenuator. The noise source is a shift register with an exclusive OR-feedback network. The feedback network has provisions to protect the shift register from being locked in the zero state.

TABLE 2. NOISE FEEDBACK CONTROL

FEEDBACK	CONFIGURATION
0	"Periodic" noise
1	"White" noise

Whenever the noise control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits. The fixed shift rates are derived from the input clock.

TABLE 3. NOISE GENERATOR FREQUENCY CONTROL

BITS		SHIFT RATE
NF0	NF1	
0	0	N/64
0	1	N/128
1	0	N/256
1	1	Tone generator #3 output

The output of the noise source is connected to a programmable attenuator as shown in Figure 4.

output buffer/amplifier

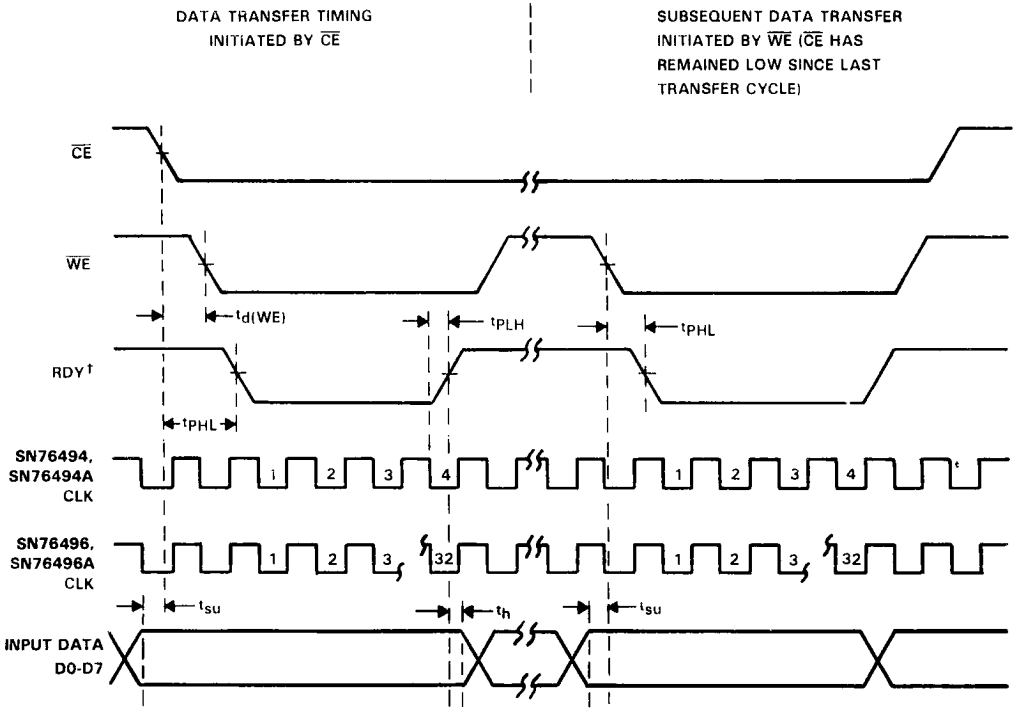
The output buffer is a conventional operational amplifier summing circuit. It sums the three tone generator outputs, the noise generator output, and any audio input through pin 9. The output buffer will generate up to 10 mA.

To prevent oscillations in the output buffer, the output (pin 7) should be decoupled. This is done by putting 10 ohms in series with 0.1 μF from pin 7 to ground (see Figure 3).

data transfer

The microprocessor selects the SN76494, SN76494A, SN76496, or SN76496A by taking $\overline{CE}$ low (low voltage). Unless $\overline{CE}$ is low, no data transfer can occur. When $\overline{CE}$ is low, the $\overline{WE}$ signal strobes the contents of the data bus to the appropriate control register. The data bus contents must be valid at this time.

The SN76494 and SN76494A require approximately 4 clock cycles to load the data into the control register. The SN76496 and SN76496A require approximately 32 clock cycles. The open-collector READY output is used to synchronize the microprocessor to this transfer and is pulled to the false state (low) immediately following the falling edge of $\overline{CE}$ (or $\overline{WE}$ when data transfer is initiated by $\overline{WE}$). READY will go high upon completion of the data transfer cycle. The data transfer timing is shown below.



† $\overline{WE}$ must be returned high (inactive) within 4 clock pulses for the SN76494 and SN76494A (32 clock pulses for the SN76496 and SN76496A) after RDY returns high. Otherwise, a new data transfer cycle will be initiated.

FIGURE 2. DATA TRANSFER TIMING

TABLE 4. FUNCTION TABLE

INPUTS		OUTPUT
$\overline{CE}$	$\overline{WE}$	READY
L	L	L
L	H	L
H	L	H
H	H	H

This table is valid when the device is:
(1) not being clocked, and
(2) is initialized by pulling $\overline{WE}$ and $\overline{CE}$ high.

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CPU interface to SN76494, SN76494A, SN76496 or SN76496A

The microprocessor interfaces with the SN76494, SN76494A, SN76496, or SN76496A by means of the 8 data lines and 3 control lines ($\overline{WE}$, $\overline{CE}$ and READY). Each tone generator requires 10 bits of information to select the frequency and four bits of information to select the attenuation. A frequency selection requires a double-byte transfer, while an attenuator selection requires a single-byte transfer.

If no other control registers on the chip are accessed, a tone generator may be rapidly updated by initially sending both bytes of frequency and register data, followed by just the second byte of data for succeeding values. The register address is latched on the chip, so the data will continue going into the same register. This allows the six most significant bits to be quickly modified for frequency sweeps.

control registers

The devices have 8 internal registers that are used to control the 3 tone generators and the noise source. During all data transfers to the devices, the first byte contains a 3-bit field that determines the destination control register. The register address codes are shown in Table 5.

TABLE 5. REGISTER ADDRESS FIELD

R0	R1	R2	DESTINATION CONTROL REGISTER
0	0	0	Tone 1 Frequency
0	0	1	Tone 1 Attenuation
0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

data formats

The formats required to transfer data are shown below.

	REG ADDR			DATA			
1	R0	R1	R2	F6	F7	F8	F9

BIT 0 FIRST BYTE BIT 7

	DATA						
0	x	F0	F1	F2	F3	F4	F5

BIT 0 SECOND BYTE BIT 7

UPDATE NOISE SOURCE (SINGLE BYTE TRANSFER)

	REG ADDR					SHIFT	
1	R0	R1	R2	x	FB	NF0	NF1

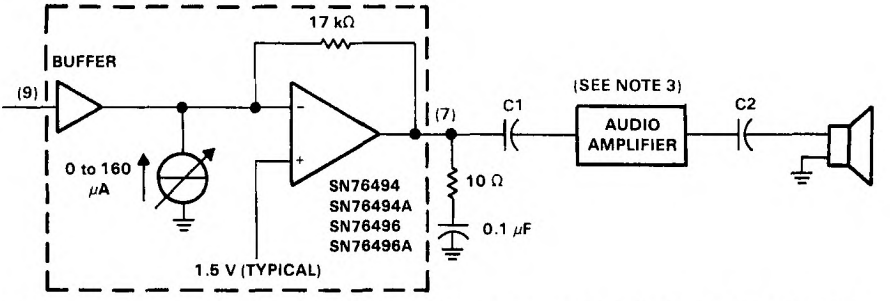
BIT 0 BIT 7

UPDATE ATTENUATOR (SINGLE BYTE TRANSFER)

	REG ADDR			DATA			
1	R0	R1	R2	A0	A1	A2	A3

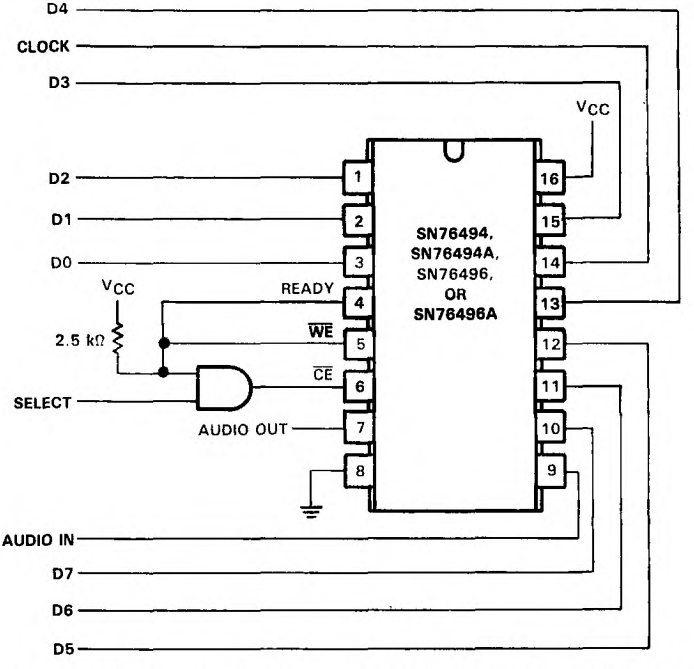
BIT 0 BIT 7

TYPICAL APPLICATION DATA



NOTE 3: The capacitance values of C1 and C2 are determined by the frequency response desired and the audio amplifier used.

FIGURE 3. EXTERNAL AUDIO OUTPUT INTERFACE



NOTES: 4. The data lines must be latched so that the data remains on them at least 32 clock cycles for the SN76496 and SN76496A or (4 clock cycles for the SN76494 and SN76494A) after the select line goes low.
5. The select pulse should be a negative-going pulse with minimum duration of 150 ns.

FIGURE 4. MICROCOMPUTER PARALLEL PORT INTERFACE

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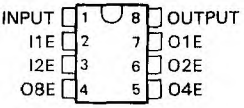
D2738, SEP ** R -REVISED APRIL 1988

- **33 Distinct Input-to-Output Emitter Ratios from 3:1 to 1:15**
- **Wide Input current Range: 1 μA to 3 mA**
- **35-Volt Output Capability**
- **High Output Impedance**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL010 is a Wilson current mirror that provides output current in a selectable fixed ratio to the input current. The ratio is substantially independent of changes in load, voltages, and temperature. Selecting the ratio consists of connecting appropriate input-emitter pins and output-emitter pins to ground as shown in Figure 1.

The TL010 is designed to operate with up to 3 mA input current if all three input-emitter pins are used. It will also operate at voltages up to 35 V.

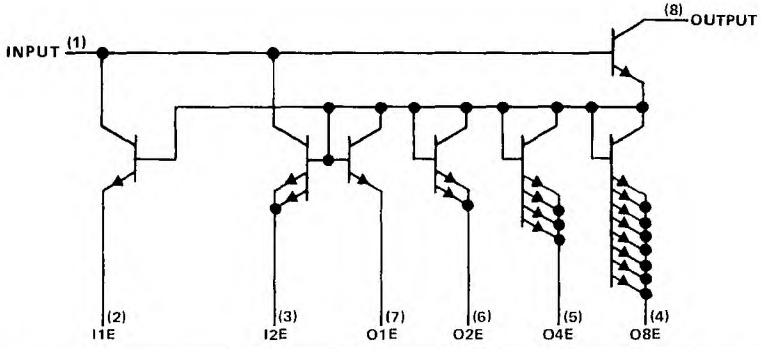
The TL010I is characterized for operation from −40°C to 85°C. The TL010C is characterized for operation from 0°C to 70°C.

typical values of current ratio at T_A = 25°C†

EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$	EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$	EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
1:15	14.1	1:6	5.78	3:8	2.61
1:14	13.2	2:11	5.34	2:5	2.43
1:13	12.3	1:5	4.82	3:7	2.26
1:12	11.4	3:14	4.53	1:2	1.98
1:11	10.5	2:9	4.38	3:5	1.64
1:10	9.55	3:13	4.21	2:3	1.45
1:9	8.62	1:4	3.89	3:4	1.32
1:8	7.72	3:11	3.57	1:1	0.99
2:15	7.23	2:7	3:40	3:2	0.663
1:7	6:71	3:10	3:25	2:1	0.50
2:13	6.29	1:3	2.90	3:1	0.332

†m is the number of input emitters used, n is the number of output emitters used.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 725 mW
Operating free-air temperature range: TL010I . . . . . −40°C to 85°C
TL010C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 8.0 mW/°C.

recommended operating conditions

	TL010I		TL010C		UNIT
	MIN	MAX	MIN	MAX	
Output voltage, V_O	5	36	5	36	V
Input voltage, V_I	0.6	1.7	0.65	1.6	V
Input current per input emitter, I_I	0.001	1	0.001	1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL010I			TL010C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_I	Input voltage	I_I = m × 1 μA			1			1		V
		I_I = m × 10 μA			1.1			1.1		
		I_I = m × 100 μA			1.25			1.25		
		I_I = m × 1 mA			1.4			1.4		
h_F	Current ratio (I_O/I_I)	I_I = MIN to MAX	m:n = 1:8	6.97	7.72	8.13	7.05	7.72	8.13	
			m:n = 1:4	3.61	3.89	4.05	3.64	3.89	4.05	
			m:n = 1:2	1.84	1.98	2.07	1.88	1.98	2.07	
			m:n = 1:1	0.89	0.99	1.08	0.94	0.99	1.04	
			m:n = 2:1	0.46	0.50	0.56	0.475	0.50	0.525	
α_{hF}	Temperature coefficient of current ratio	I_I = MIN to MAX			300			300		ppm/°C
	Output-to-input isolation	I_I = MIN to MAX,	f = 1 kHz	60			60			dB
$V_{O(th)}$	Output threshold voltage§	I_I = MIN to MAX	T_A = [illegible]			1.1			1.05	V
			T_A = [illegible]			1			1	
r_o	Output resistance¶	F = 1 kHz	I_I = m × 10 μA		200 m/n			200 m/n		MΩ
			I_I = m × 100 μA		20 m/n			20 m/n		
			I_I = m × 1 mA		2 m/n			2 m/n		
f_{max}	Maximum operating frequency#	I_I = m × 1 mA, R_L = 500 Ω			10			10		MHz

† m is the number of input emitters, n is the number of output emitters. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C.
§Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶The output resistance is directly proportional to the number of input emitters divided by the number of output emitters (m/n).
#Maximum operating frequency is the frequency at which the output current is down 3 dB from its low-frequency value.

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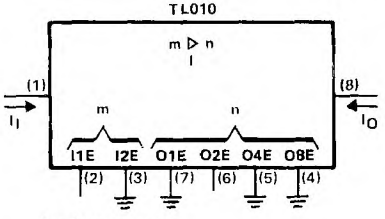
TYPICAL APPLICATION INFORMATION



See Notes 3 and 4

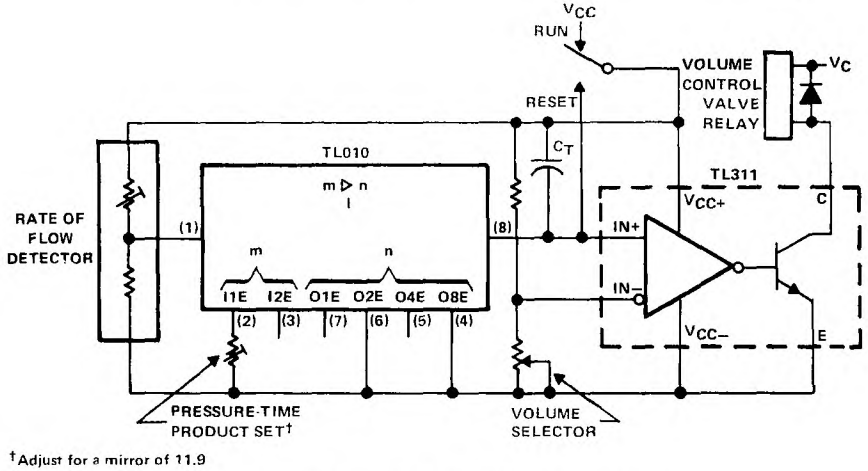
NOTES: 3. Selected emitters must be grounded as close as possible to the package to avoid unstable device behavior.
Using the fixed-Beta model, the current ratio for a current mirror of m input emitters and n output emitters may be calculated as

$$\frac{I_O}{I_I} = \frac{\beta^2 n + \beta(n + m)}{\beta^2 m + (\beta + 1)(m + n)}$$

Second-order effects, such as on-chip self-heating, may slightly perturb the observed ratio from the calculated value.

4. At high current levels, a small capacitor (270 pF) may be required between the input and output terminals to improve stability.

FIGURE 1. CURRENT MIRROR SET FOR A CURRENT RATIO OF 2:13



†Adjust for a mirror of 11.9

FIGURE 2. TYPICAL APPLICATION CIRCUIT

In the application shown in Figure 2, the problem is to measure a precise volume of liquid flowing through a line and shut off the flow with a relay when limit is reached. For the particular volume to be measured and the pressure detector used, a current gain of 11.9 is required. By setting the TL010 for a gain of 10 with the emitter selection, the exact gain of 11.9 may be obtained by adjusting the pressure-time product control.

D2614, FEBRUARY 1984—REVISED OCTOBER 1988

- **Wide Input Current Range:**
  1 μA to 1 mA
- **35-Volt Output Capability**
- **High Output Impedance**
- **Current-Ratio Tolerances Over Full Temperature Range;**
  ±8% for I Suffix
  ±7% for C Suffix
- **Typically Less Than ±1% Error at 25°C**

LP PACKAGE
(TOP VIEW)

TEMPERATURE RANGE	INPUT-TO-OUTPUT CURRENT RATIO			
	1:1	1:2	1:4	2:1
−40°C to 85°C	TL011I	TL012I		TL021I
0°C to 70°C	TL011C	TL012C	TL014AC	TL021C

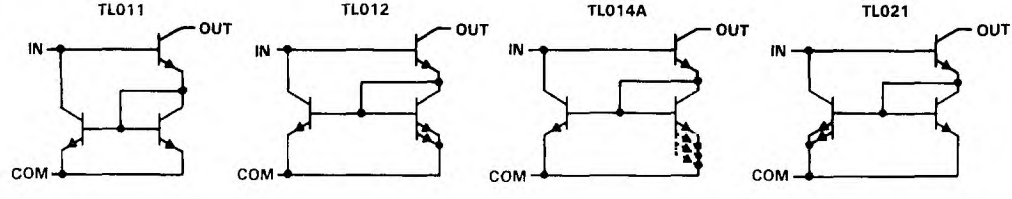
description

The TL011, TL012, TL014A, and TL021 are Wilson current mirrors with output currents in fixed proportion to the input currents and substantially independent of changes in voltage, load, and temperature. These devices make use of the tight matching properties of identical bipolar transistors on a monolithic integrated circuit chip to achieve current-ratio accuracy typically better than 98%.

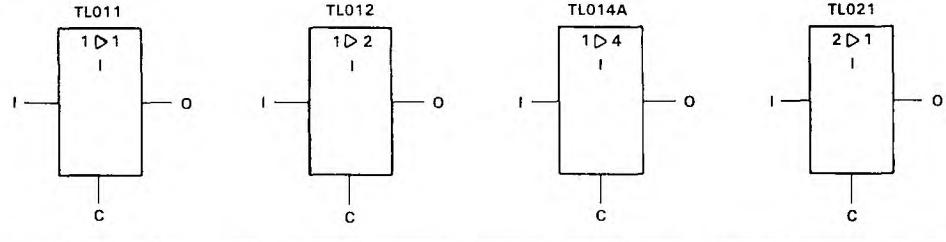
Current mirrors are used extensively in linear integrated circuit designs as active loads for operational-amplifier stages and as current sources for other stages. The TL011 family gives the designer this same capability with no sacrifice in accuracy or stability.

The TL011, TL012, and TL014A are designed to operate with input currents up to 1 mA and output voltage up to 35 V. The TL021 is designed for 2 mA and 35 V.

schematics



symbols



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 775 mW
Operating free-air temperature range: TL011I, TL012I, TL021I . . . . . −40°C to 85°C
TL011C, TL012C, TL014AC, TL021C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C. The LP package dissipation rating was based on thermal resistance, $R_{\theta JA}$, measured in still air with the device mounted in an Augat socket. The bottom of the package was 10 mm (0.375 in.) above the socket.

recommended operating conditions

		TL0__I		TL0__C, AC		UNIT
		MIN	MAX	MIN	MAX	
Output voltage, V_O		5	35	5	35	V
Input current, I_O	TL011	0.002	2	0.002	2	mA
	All others	0.001	1	0.001	1	
Operating free-air temperature, T_A		−40	85	0	70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL011			TL012			TL014A			TL021			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_I	Input voltage		I_I = 1 μA			1			1			1					V
			I_I = 2 μA												1		
			I_I = 10 μA			1.1			1.1			1.1					
			I_I = 20 μA												1.1		
			I_I = 100 μA			1.25			1.25			1.25					
			I_I = 200 μA												1.25		
			I_I = 1 mA			1.4			1.4			1.4					
			I_I = 2 mA												1.4		
h_F	Current ratio (I_O/I_I)	TLO_I	I_I = MIN to MAX‡		0.92	1	1.08	1.84	2	2.16	3.68	4	4.32	0.46	0.5	0.54	
		TLO_C, AC			0.93	1	1.07	1.86	2	2.14	3.72	4	4.28	0.465	0.5	0.535	
α_{hF}	Temperature coefficient of current ratio		I_I = MIN to MAX			50			100			200			200		ppm/°C
	Output-to-input isolation		I_I = MIN to MAX,	f = 1 kHz	80			80			80			80			dB
$V_{O(th)}$	Output threshold voltage§	TLO_I	I_I = MIN to MAX	T_A = −40°C			1.35			1.35			1.35			1.35	V
		TLO_C, AC		T_A = 0°C			1.25			1.25			1.25			1.25	
		All		T_A = 25°C			1.2			1.2			1.2			1.2	
r_o	Output resistance		f = 1 kHz	I_I = 10 μA		200			100			50					MΩ
				I_I = 20 μA											200		
				I_I = 100 μA		20			10			5					
				I_I = 200 μA											20		
				I_I = 1 mA		2			1			0.5					
				I_I = 2 mA											2		
f_{max}	Maximum operating frequency¶		I_I = MAX	R_L = 500 Ω		10			10			10			10		MHz

†All typical values are at T_A = 25°C.
‡For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
§Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶Maximum operating frequency is the frequency at which the output current is down 3 dB from its low frequency value.

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TYPICAL CHARACTERISTICS

TL011
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

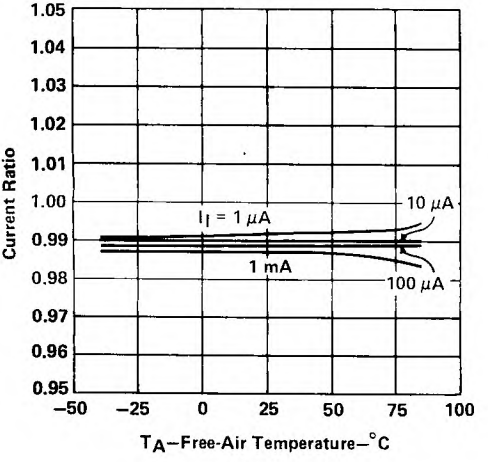

FIGURE 1

TL012
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

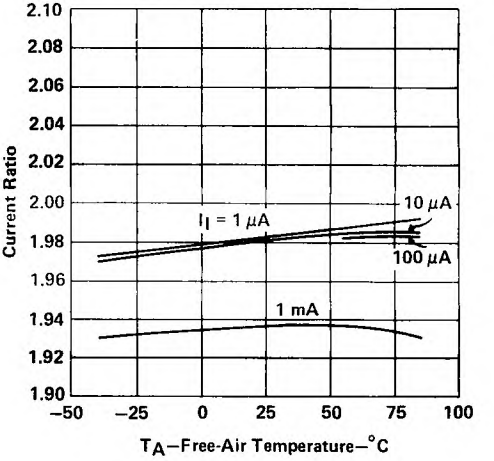

FIGURE 2

TL014A
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

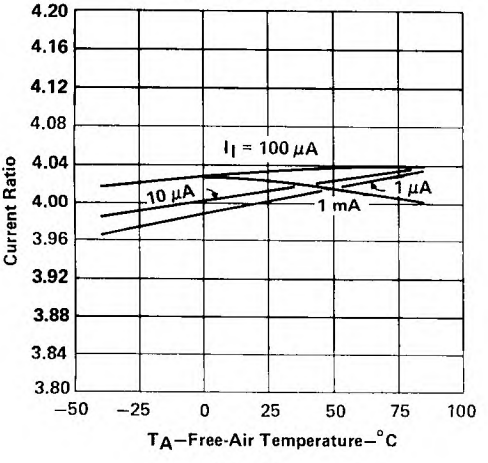

FIGURE 3

TL021
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

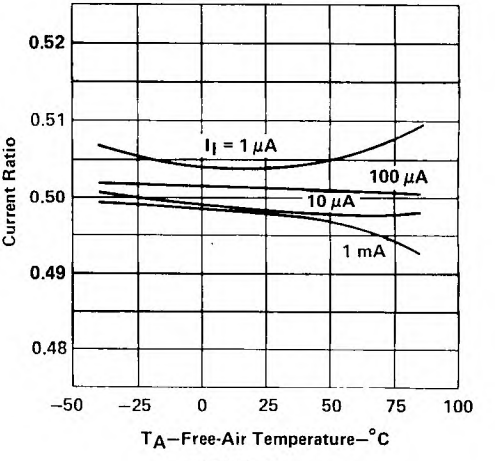

FIGURE 4

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TYPICAL APPLICATIONS INFORMATION

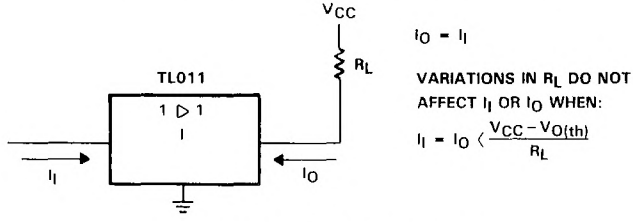
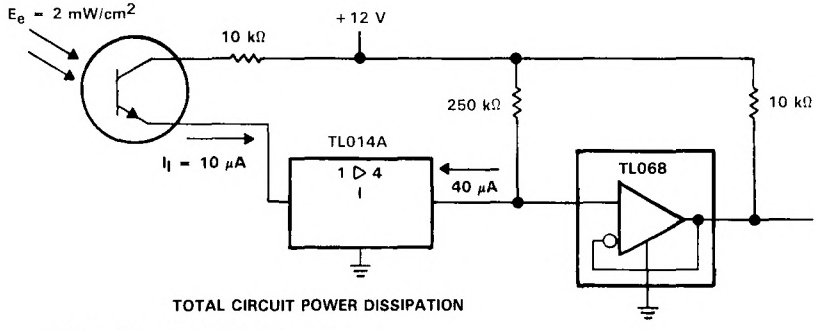


FIGURE 5. BASIC CURRENT BUFFER



TOTAL CIRCUIT POWER DISSIPATION

Idle condition: P_D = 1.5 mW typical
On condition: P_D = 12.5 mW typical
10 μA from phototransistor provides a V_O swing of 10 V at 1 mA.

FIGURE 6. PHOTOTRANSISTOR PREAMPLIFIER

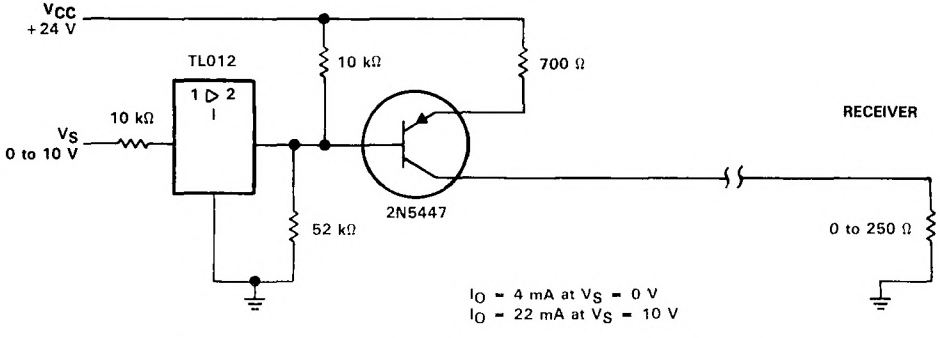
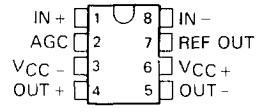


FIGURE 7. TWO-WIRE LINEAR CURRENT-MODE TRANSMITTER

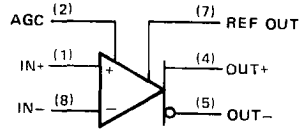
D2790, JUNE 1985—REVISED OCTOBER 1988

- Low Output Common-Mode Sensitivity to AGC Voltages
- Input and Output Impedances Independent of AGC Voltage
- Peak Gain . . . 38 dB Typ
- Wide AGC Range . . . 50 dB Typ
- 3-dB Bandwidth . . . 50 MHz
- Other Characteristics Similar to NE592 and uA733

D OR P PACKAGE
(TOP VIEW)



symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pin. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers where a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL026C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	ABOVE $T_A = 25°C$ DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at 25 °C operating free-air temperature, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	65	85	105	V/V
ΔA_{VD}	Change in voltage amplification	1	V_{IPP} = 28.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV		−50		dB
V_{ref}	Voltage at REF OUT		I_{ref} = −1 mA to 100 μA	1.3		1.5	V
	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V, $V_{AGC} - V_{ref}$ = ±180 mV		50		MHz
I_{IO}	Input offset current				0.4	5	μA
I_{IB}	Input bias current				10	30	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} = 0 to 2 V, R_L = ∞			300	mV
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞			0.75	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	3	4		V
r_i	Input resistance at AGC, IN+, or IN−			10	30		kΩ
r_o	Output resistance				20		Ω
CMRR	Common-mode rejection ratio	3 3	V_{IC} = ±1 V, f = 100 kHz V_{IC} = ±1 V, f = 5 mHz	60	86 60		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		6	10	ns
t_r	Rise time	2	ΔV_O = 1 V		4.5	12	ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	3	4		mA
I_{CC}	Supply current		No load, No signal		22	27	mA

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electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	55		115	V/V
I_{IO}	Input offset current					6	μA
I_{IB}	Input bias current					40	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞			1.5	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	2.8			V
r_i	Input resistance at AGC, IN+, or IN−			8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal			30	mA

PARAMETER MEASUREMENT INFORMATION

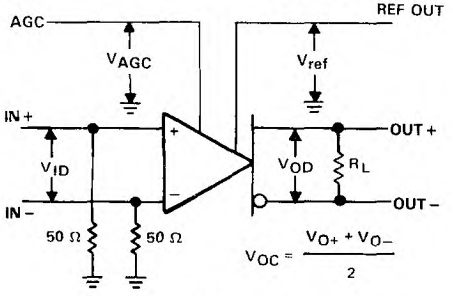

FIGURE 1

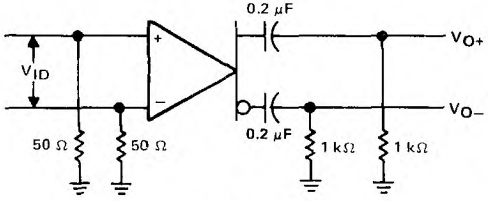

FIGURE 2

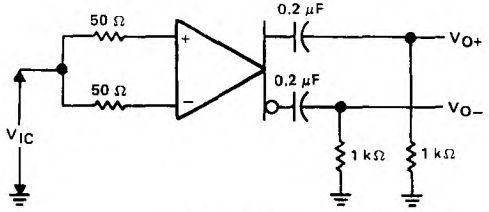

FIGURE 3

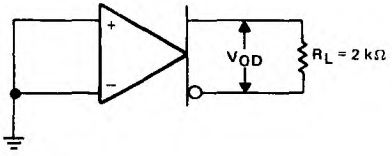

FIGURE 4

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

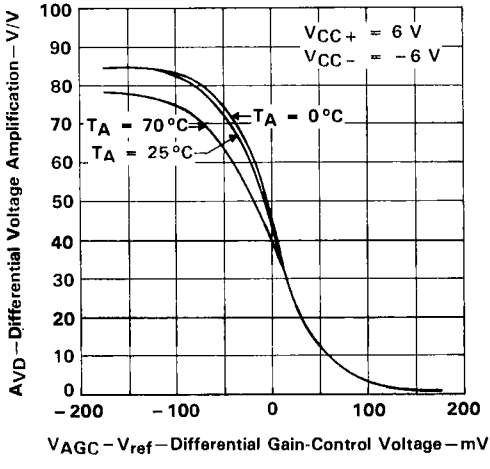

FIGURE 5

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TYPICAL APPLICATION INFORMATION

gain characteristics

Figure 5 shows the differential voltage amplification versus the differential gain-control voltage ($V_{AGC} - V_{ref}$). V_{AGC} is the absolute voltage applied to the AGC input and V_{ref} is the dc voltage at the REF OUT output. As V_{AGC} increases with respect to V_{ref}, the TL026C gain changes from maximum to minimum. As shown in Figure 5 for example, V_{AGC} would have to vary from approximately 180 mV less than V_{ref} to approximately 180 mV greater than V_{ref} to change the gain from maximum to minimum. The total signal change in V_{AGC} is defined by the following equation.

$$\Delta V_{AGC} = V_{ref} + 180\ mV - (V_{ref} - 180\ mV) \quad (1)$$

$$\Delta V_{AGC} = 360\ mV$$

However, because V_{AGC} varies as the ac AGC signal varies and also differentially around V_{ref}, then V_{AGC} should have an ac signal component and a dc component. To preserve the dc and thermal tracking of the device, this dc voltage must be generated from V_{ref}. To apply proper bias to the AGC input, the external circuit used to generate V_{AGC} must combine these two voltages. Figures 6 and 7 show two circuits that will perform this operation and are easy to implement. The circuits use a standard dual operational amplifier for AGC feedback. By providing rectification and the required feedback gain, these circuits are also complete AGC systems.

circuit operation

Amplifier A1 amplifies and inverts the rectified and filtered AGC signal voltage V_C producing output voltage V1. Amplifier A2 is a differential amplifier that inverts V1 again and adds the scaled V_{ref} voltage. This conditioning makes V_{AGC} the sum of the signal plus the scaled V_{ref}. As the signal voltage increases, V_{AGC} increases and the gain of the TLC026C is reduced. This maintains a constant output level.

feedback circuit equations

Following the AGC input signal (Figures 6 and 7) from the OUT output through the feedback amplifiers to the AGC input produces the following equation:

1. AC output to diode D1, assuming sinusoidal signals

$$V_O = V_{OP}(\sin(wt)) \quad (2)$$

where:

V_{OP} = peak voltage of V_O

2. Diode D1 and capacitor C1 output

$$V_C = V_{OP} - V_F \quad (3)$$

where:

V_F = forward voltage drop of D1
V_C = voltage across capacitor C1

3. A1 output

$$V1 = -\frac{R2}{R1} V_C \quad (4)$$

TYPICAL APPLICATION INFORMATION

4. A2 output (R3 = R4)

$$V_{AGC} = \frac{R2}{R1} V_c + 2 \frac{R6}{R5 + R6} V_{ref} \quad (5)$$

Amplifier A2 inverts V1 producing a positive AGC signal voltage. Therefore, the input voltage to the TL026C AGC pin consists of an AGC signal equal to:

$$\frac{R2}{R1} V_c \quad (6)$$

and a dc voltage derived from V_{ref}, defined as the quiescent value of V_{AGC}.

$$V_{AGC(q)} = 2 \frac{R6}{R5 + R6} V_{ref} \quad (7)$$

For the initial resistor calculations, V_{ref} is assumed to be typically 1.4 V making quiescent V_{AGC} approximately 1.22 V ($V_{AGC(q)} = V_{ref} - 180$ mV). This voltage allows the TL026C to operate at maximum gain under no-signal and low-signal conditions. In addition, with V_{ref} used as both internal and external reference, its variation from device to device automatically adjusts the overall bias and makes AGC operation essentially independent of the absolute value of V_{ref}. The resistor divider needs to be calculated only once and is valid for the full tolerance of V_{ref}.

output voltage limits (see Figures 6 and 7)

The output voltage level desired must fall within the following limits.

1. Because the data sheet minimum output swing is 3 V peak-to-peak using a 2-kΩ load resistor, the user-selected design limit for the peak output swing should not exceed 1.5 V.
2. The voltage drop of the rectifying diode determines the lower voltage limit. When a silicon diode is used, this voltage is approximately 0.7 V. The output voltage V_o must have sufficient amplitude to exceed the rectifying diode drop. A schottky diode can be used to reduce the V_o level required.

gain calculations for a peak output voltage of 1 V

A peak output voltage of 1 V was chosen for gain calculations because it is approximately midway between the limits of conditions 1 and 2 in the preceding paragraph.

Using equation 3 ($V_c = V_{OP} - V_d$), V_c is calculated as follows:

$$V_c = 1 \text{ V} - 0.7 \text{ V}$$

$$V_c = 0.3 \text{ V}$$

Therefore, the gain of A1 must produce a voltage V1 that is equal to or greater than the total change in V_{AGC} for maximum TL026C gain change.

With a total change in V_{AGC} of 360 mV and using equation 4, the calculation is as follows:

$$-\frac{V1}{V_c} = \frac{\Delta V_{AGC}}{V_c} = \frac{R2}{R1} = \frac{0.36}{0.3} = 1.2$$

If R1 is 10 kΩ, R2 is 1.2 times R1 or 12 kΩ.

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TYPICAL APPLICATION INFORMATION

Since the output voltage for this circuit must be between 0.85 V and 1.3 V, the component values in Figures 6 and 7 provide a nominal 1-V peak output limit. This limit is the best choice to allow for temperature variations of the diode and minimum output voltage specification.

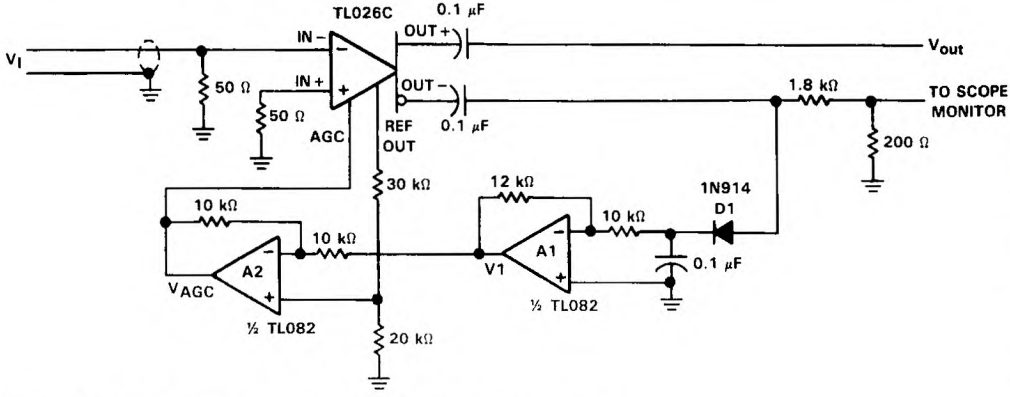
The circuit values in Figures 6 and 7 will produce the best results in this general application. Because of rectification and device input constraints, the circuit in Figure 6 will not provide attenuation and has about 32 dB of control range. The circuit shown in Figure 7 will have approximately 25% variation in the peak output voltage limit due to the variation in gain of the TL592 device to device. In addition, if a lower output voltage is desired, the output of the TL026C can be used for approximately 40 mV of controlled signal.

considerations for the use of the TL026C

To obtain the most reliable results, RF breadboarding techinques must be used. A groundplane board should be used and power supplies should be bypassed with 0.1-μF capacitors. Input leads and output leads should be as short as possible and separated from each other.

A peak input voltage greater than 200 mV will begin to saturate the input stages of the TL026C and, while the circuit is in the AGC mode, the output signal may become distorted.

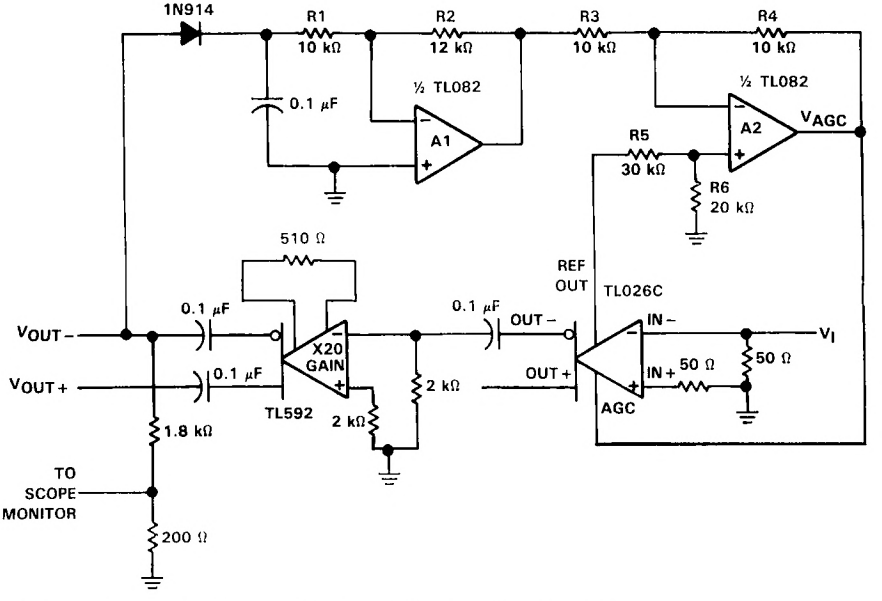
To observe the output signal of TL026C or TL592, low-capacitance FET probes or the output voltage divider technique shown in Figure 6 should be used.



NOTE: V_{CC+} = 6 V and V_{CC-} = −6 V for TL026C and amplifiers A1 and A2.

FIGURE 6. TYPICAL APPLICATION CIRCUIT WITH NO ATTENUATION

TYPICAL APPLICATION INFORMATION



NOTE: V_{CC+} = 6 V and V_{CC-} = −6 V for TL026C and amplifiers A1 and A2.

FIGURE 7. TYPICAL APPLICATION CIRCUIT WITH ATTENUATION

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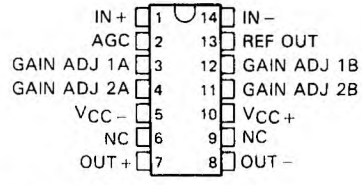
D2888, JUNE 1985—REV JANUARY 1989

- **Low Output Common-Mode Sensitivity to AGC Voltages**
- **Input and Output Impedances Independent of AGC Voltage**
- **Wide AGC Range . . . 50 dB Typ**
- **3-dB Bandwidth . . . 50 MHz**
- **Other Characteristics Similar to NE592 and uA733**

D, J, OR N PACKAGE
(TOP VIEW)

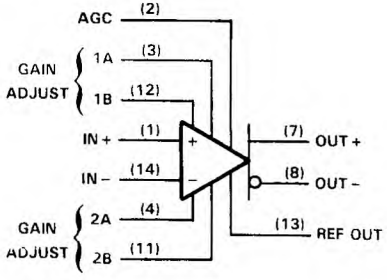


NC No internal connection

DEVICE FEATURES

	GAIN	AGC
Gain Option 1	50 dB	50 dB
Gain Option 2	38 dB	50 dB

symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pins. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers for which a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL027M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL027C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . 500 mW
Operating free-air temperature: TL027M . . . . . −55°C to 125°C
TL027C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		3	6	8	V
Supply voltage, V_{CC-}		−3	−6	−8	V
Operating free-air temperature, T_A	TL027M	−55		125	°C
	TL027C	0		70	

electrical characteristics at 25°C operating free-air temperature, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	200		400	V/V
				2	65	85	105	
ΔA_{VD1}	Change in voltage amplification	1	$V_{I(PP)}$ = 7.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV	1		−50		dB
ΔA_{VD2}	Change in voltage amplification	1	$V_{I(PP)}$ = 28.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV	2		−50		dB
V_{ref}	Voltage at REF OUT		I_{ref} = 1 mA to 100 μA	1	1.3		1.5	V
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V, $V_{AGC} - V_{ref}$ = ±180 mV	1		20		MHz
				2		50		
I_{IO}	Input offset current			1 or 2		0.4	5	μA
I_{IB}	Input bias current			1 or 2		10	30	μA
V_{ICR}	Common-mode input voltage range	3		2	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1 or 2	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} = 0 to 2 V, R_L = ∞	1 or 2			300	mV
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			0.75	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	3	4		V
r_i	Input resistance			1		4		kΩ
				2	10	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f < 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	1 or 2		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = ±1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = ±1 V	1		10.5		ns
				2		4.5	12	
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	3	4		mA
I_{CC}	Supply current		No load, No signal	1 or 2		22	27	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

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electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0 V, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	150		450	V/V
				2	55		115	
I_{IO}	Input offset current			1 or 2			6	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	2.8			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f < 100 kHz	2	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal	1 or 2			30	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

PARAMETER MEASUREMENT INFORMATION

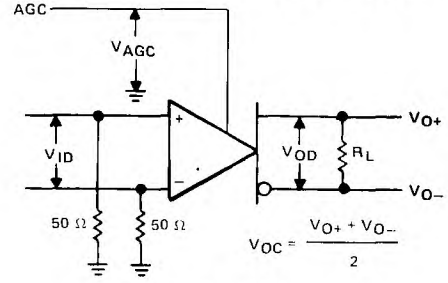

FIGURE 1

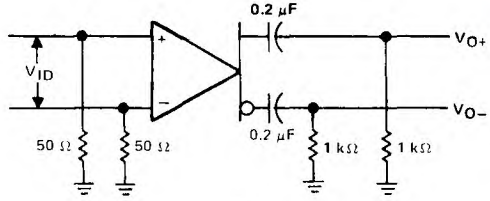

FIGURE 2

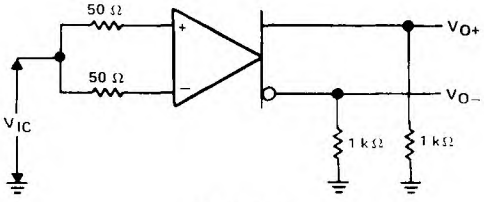

FIGURE 3

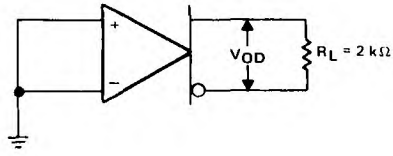

FIGURE 4

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

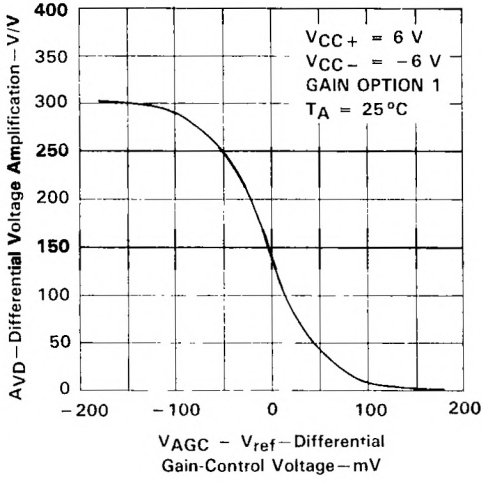

FIGURE 5

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

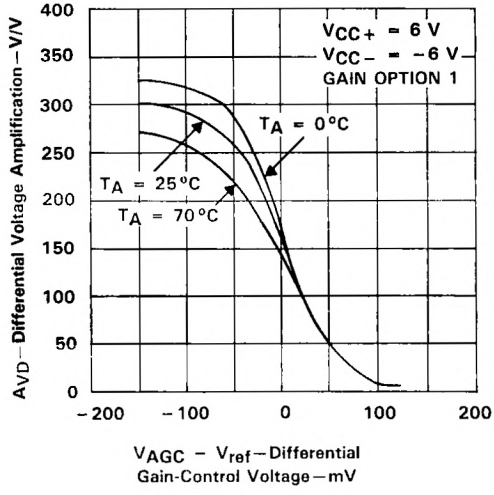

FIGURE 6

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TYPICAL APPLICATION INFORMATION

gain characteristics

Figure 5 and 6 show the differential voltage amplification versus the differential gain-control voltage ($V_{AGC} - V_{ref}$). V_{AGC} is the absolute voltage applied to the AGC input and V_{ref} is the dc voltage at the REF OUT output. As V_{AGC} increases with respect to V_{ref}, the TL027C gain changes from maximum to minimum. As shown in Figure 5 for example, V_{AGC} would have to vary from approximately 180 mV less than V_{ref} to approximately 180 mV greater than V_{ref} to change the gain from maximum to minimum. The total signal change in V_{AGC} is defined by the following equation.

$$\Delta V_{AGC} = V_{ref} + 180\ mV - (V_{ref} - 180\ mV) \quad (1)$$

$$\Delta V_{AGC} = 360\ mV$$

However, because V_{AGC} varies as the ac AGC signal varies and also differentially around V_{ref}, then V_{AGC} should have an ac signal component and a dc component. To preserve the dc and thermal tracking of the device, this dc voltage must be generated from V_{ref}. To apply proper bias to the AGC input, the external circuit used to generate V_{AGC} must combine these two voltages. Figures 7 and 8 show two circuits that will perform this operation and are easy to implement. The circuits use a standard dual operational amplifier for AGC feedback. By providing rectification and the required feedback gain, these circuits are also complete AGC systems.

circuit operation

Amplifier A1 amplifies and inverts the rectified and filtered AGC signal voltage V_C producing output voltage V1. Amplifier A2 is a differential amplifier that inverts V1 again and adds the scaled V_{ref} voltage. This conditioning makes V_{AGC} the sum of the signal plus the scaled V_{ref}. As the signal voltage increases, V_{AGC} increases and the gain of the TLC027C is reduced. This maintains a constant output level.

feedback circuit equations

Following the AGC input signal (Figures 7 and 8) from the OUT − output through the feedback amplifiers to the AGC input produces the following equations.

1. AC output to diode D1, assuming sinusoidal signals

$$V_O = V_{OP}\ (\sin\ (wt)) \quad (2)$$

where:

V_{OP} = peak voltage of V_O

2. Diode D1 and capacitor C1 output

$$V_C = V_{OP} - V_F \quad (3)$$

where:

V_F = forward voltage drop of D1
V_C = voltage across capacitor C1

3. A1 output

$$V1 = -\frac{R2}{R1} V_C \quad (4)$$

TYPICAL APPLICATION INFORMATION

4. A2 output (R3 = R4)

$$V_{AGC} = \frac{R2}{R1} V_c + 2 \frac{R1}{R5 + R6} V_{ref} \quad (5)$$

Amplifier A2 inverts V1 producing a positive AGC signal voltage. Therefore, the input voltage to the TL027C AGC pin consists of an AGC signal equal to:

$$\frac{R2}{R1} V_c \quad (6)$$

and a dc voltage derived from V_{ref}, defined as the quiescent value of V_{AGC}.

$$V_{AGC(q)} = 2 \frac{R6}{R5 + R6} V_{ref} \quad (7)$$

For the initial resistor calculations, V_{ref} is assumed to be typically 1.4 V making quiescent V_{AGC} approximately 1.22 V ($V_{AGC(q)} = V_{ref} - 180$ mV). This voltage allows the TL027C to operate at maximum gain under no-signal and low-signal conditions. In addition, with V_{ref} used as both internal and external reference, its variation from device to device automatically adjusts the overall bias and makes AGC operation essentially independent of the absolute value of V_{ref}. The resistor divider needs to be calculated only once and is valid for the full tolerance of V_{ref}.

output voltage limits (see Figures 7 and 8)

The output voltage level desired must fall within the following limits:

1. Because the data sheet minimum output swing is 3 V peak-to-peak using a 2-kΩ load resistor, the user-selected design limit for the peak output swing should not exceed 1.5 V.
2. The voltage drop of the rectifying diode determines the lower voltage limit. When a silicon diode is used, this voltage is approximately 0.7 V. The output voltage V_O must have sufficient amplitude to exceed the rectifying diode drop. A schottky diode can be used to reduce the V_O level required.

gain calculations for a peak output voltage of 1 V

A peak output voltage of 1 V was chosen for gain calculations because it is approximately midway between the limits of conditions 1 and 2 in the preceding paragraph.

Using equation 3 ($V_c = V_{OP} - V_d$), V_c is calculated as follows:

$$V_c = 1 \text{ V} - 0.7 \text{ V}$$

$$V_c = 0.3 \text{ V}$$

Therefore, the gain of A1 must produce a voltage V1 that is equal to or greater than the total change in V_{AGC} for maximum TL027C gain change.

With a total change in V_{AGC} of 360 mV and using equation 4, the calculation is as follows:

$$-\frac{V1}{V_c} = \frac{\Delta V_{AGC}}{V_c} = \frac{R2}{R1} = \frac{0.36}{0.3} = 1.2$$

If R1 is 10 kΩ, R2 is 1.2 times R1 or 12 kΩ.

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TYPICAL APPLICATION INFORMATION

Since the output voltage for this circuit must be between 0.85 V and 1.3 V, the component values in Figures 7 and 8 provide a nominal 1-V peak output limit. This limit is the best choice to allow for temperature variations of the diode and minimum output voltage specification.

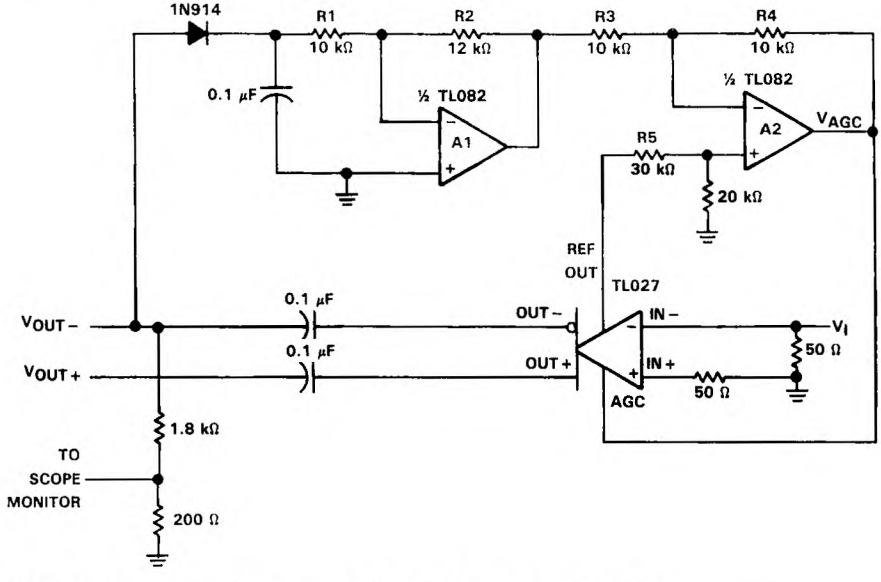
The circuit values in Figures 7 and 8 will produce the best results in this general application. Because of rectification and device input constraints, the circuit in Figure 7 will not provide attenuation and has about 32 dB of control range. The circuit shown in Figure 8 will have approximately 25% variation in the peak output voltage limit due to the variation in gain of the TL592 device to device. In addition, if a lower output voltage is desired, the output of the TL027C can be used for approximately 40 mV of controlled signal.

considerations for the use of the TL027C

To obtain the most reliable results, RF breadboarding techinques must be used. A groundplane board should be used and power supplies should be bypassed with 0.1-μF capacitors. Input leads and output leads should be as short as possible and separated from each other.

A peak input voltage greater than 200 mV will begin to saturate the input stages of the TL027C and, while the circuit is in the AGC mode, the output signal may become distorted.

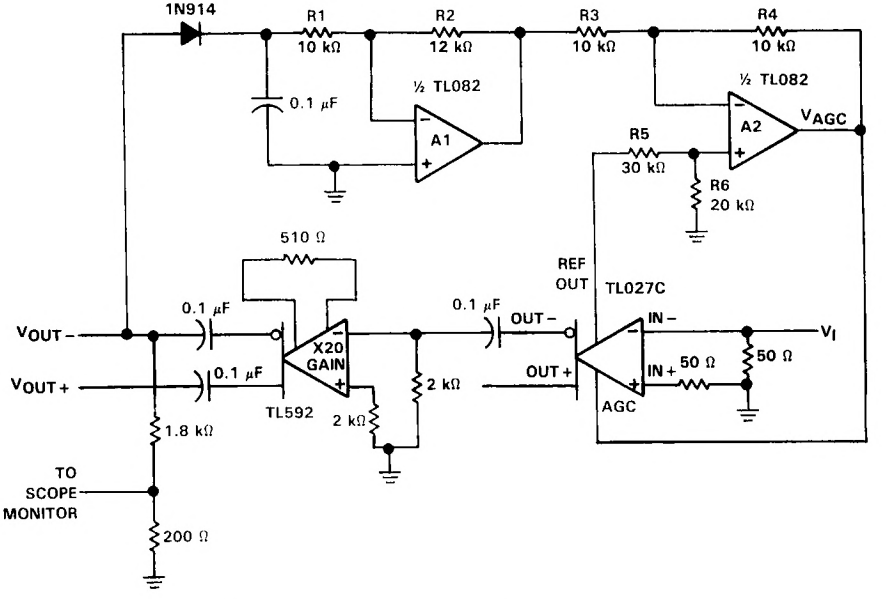
To observe the output signal of TL027C or TL592, low-capacitance FET probes or the output voltage divider technique shown in Figure 7 should be used.



NOTES: A. V_{CC+} = 6 V and V_{CC-} = −6 V for TL027C and amplifiers A1 and A2.
B. On the TL027, short pin 3 to pin 12 and pin 4 to pin 11. Connect pins 6 and 9 to ground.

FIGURE 7. TYPICAL APPLICATION CIRCUIT WITH NO ATTENUATION

TYPICAL APPLICATION INFORMATION



NOTES: A. V_{CC+} = 6 V and V_{CC-} = −6 V for TL027C and amplifiers A1 and A2.
B. On TL027, short pin 3 to pin 12 and pin 4 to pin 11. Connect pins 6 and 9 to ground.

FIGURE 8. TYPICAL APPLICATION CIRCUIT WITH ATTENUATION

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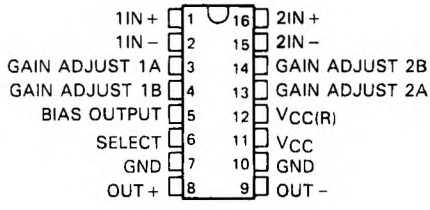
... MAR...-1988 RE...-DECEMBER 1988

- **Designed for Use with the TL041 Magnetic Field Pulse Detector**
- **Wide Bandwidth . . . 20 MHz Typ**
- **Low Noise . . . Less than 8 μV Typ**
- **Independently Adjustable Channel Gains . . . Up to 450 Typ**
- **No Frequency Compensation Required**
- **Internal Voltage Source Eliminates External Components**
- **Input Channel Select Pin is Compatible with TTL and CMOS**
- **Low Power Dissipation . . . 150 mW Typ**

D OR N PACKAGE
(TOP VIEW)



CHANNEL SELECT TABLE

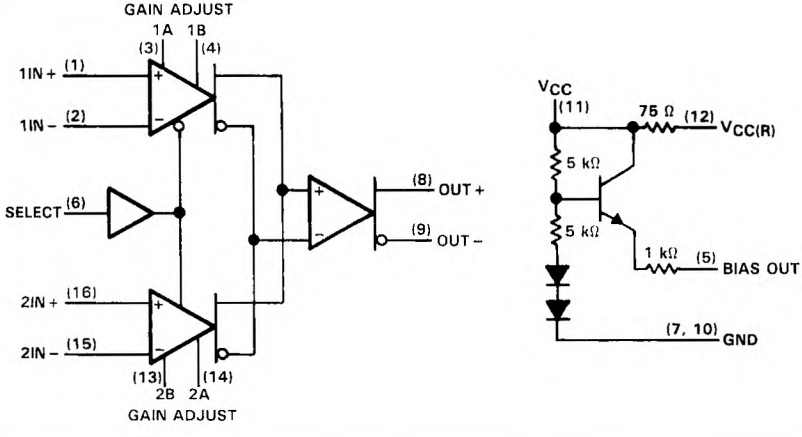
SELECT	CHANNEL
L	1
H	2

description

The TL040 is a two-channel multiplexed video amplifier designed for use with magnetic pulse detectors in streaming tape drives. The circuit design eliminates many external components, and the D package allows substantial reduction in circuit board area. The gain of each channel is a function of the resistance across its gain-adjust pins (A-B) with maximum gain occurring when the terminals are shorted.

The $V_{CC(R)}$ pin provides supply voltage decoupling required by some designs. The BIAS OUT pin provides a voltage source for other circuits that is approximately equal to 1/2 V_{CC}.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) . . . . . 14 V
Input voltage range . . . . . −0.2 V to V_{CC} + 0.2 V
Continuous total power dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages except differential voltages are with respect to the ground terminals.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	10.8	12	13.2	V
Common-mode input voltage nputs), V_{IC}	5	6	7	V
High-level input voltage, SELECT input, V_{IH}	2			V
Low-level input voltage, SELECT input, V_{IL}			0.8	V
Output sink current (diff outputs), I_{sink}			1.5	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics of selected channel at T_A = 25°C, V_{CC} = 12 V, R_{AB} = 0, R_L = 2 kΩ (unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1		300	530	600	V/V
	Channel amplification mismatch	1			1%		
	Large-signal differential voltage attenuation	1	Δ V_I = 50 mV on unselected input		60		dB
V_{OC}	Common-mode output voltage	1	R_L = ∞		8.5		V
V_{OPP}	Maximum peak-to-peak output voltage swing	1			4		V
BW	Bandwidth (−3 dB)	2			20		MHz
I_{IO}	Input offset current	1			0.1	3	μA
I_{IB}	Input bias current	1			6	17	μA
V_{OD}	Differential output voltage	1	R_L = ∞, V_{ID} = 0		0.2		V
r_i	Input resistance (differential inputs)				4		kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = 5 V to 7 V	60	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	V_{CC} = 10.8 V to 13.2 V	50	70		dB
V_n	Broadband equivalent input noise voltage	4			<5		μV
I_{IH}	High-level input current, Select input		V_{IH} = 2.7 V			−0.4	mA
I_{IL}	Low-level input current, Select input		V_{IL} = 0.4 V			20	μA
t_{pd}	Propagation delay time (differential inputs)	2	ΔV_O = 1 V		15		ns
t_r	Output rise time	2	ΔV_O = 1 V		20		ns
I_{CC}	Supply current	1			12	15	mA
	Bias output voltage	1		5	6	7	V

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PARAMETER MEASUREMENT INFORMATION

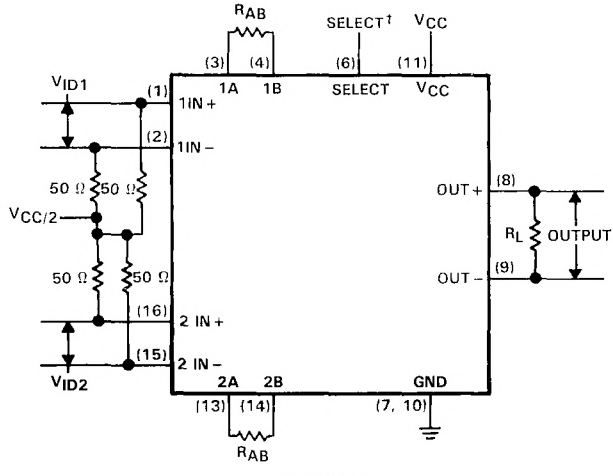

FIGURE 1

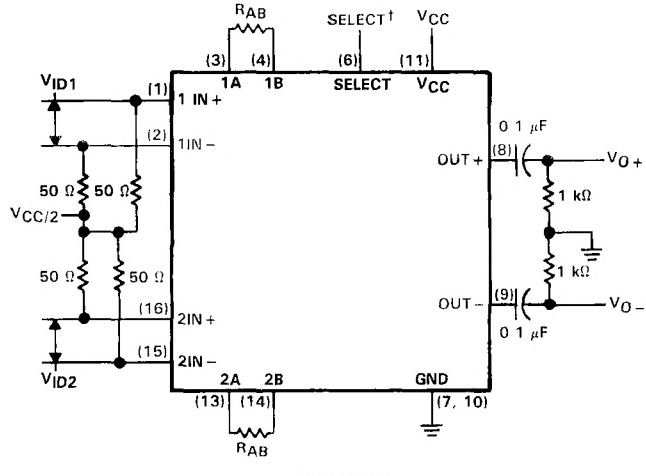

FIGURE 2

†Select input must be at proper logic level to select desired input channel.

PARAMETER MEASUREMENT INFORMATION (continued)

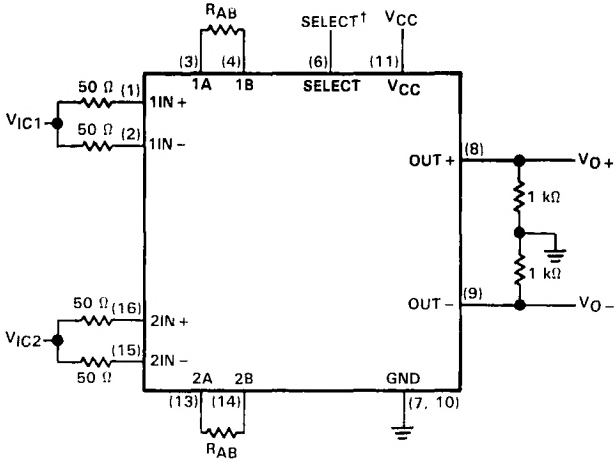

FIGURE 3

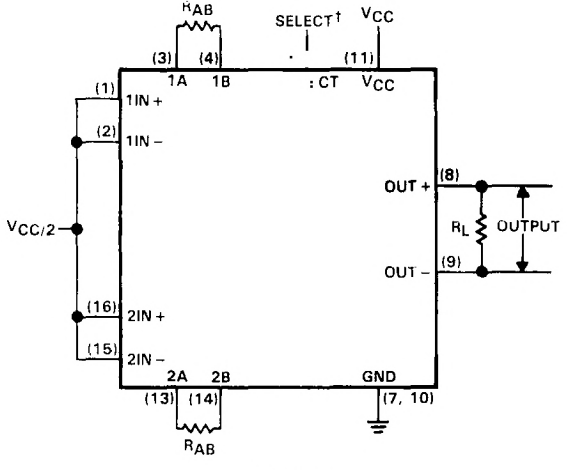

FIGURE 4

†Select input must be at proper logic level to select desired input channel.

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TYPICAL CHARACTERISTICS

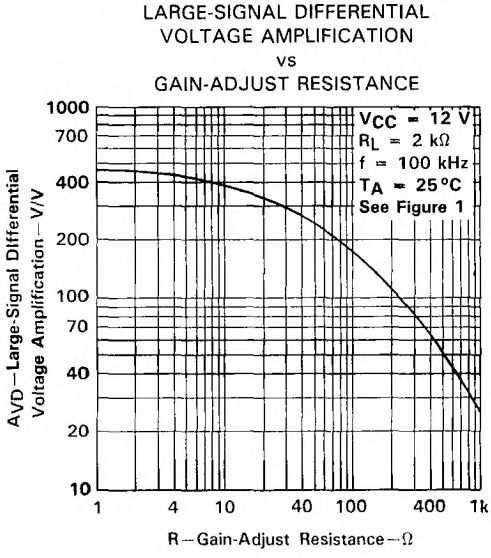


FIGURE 5

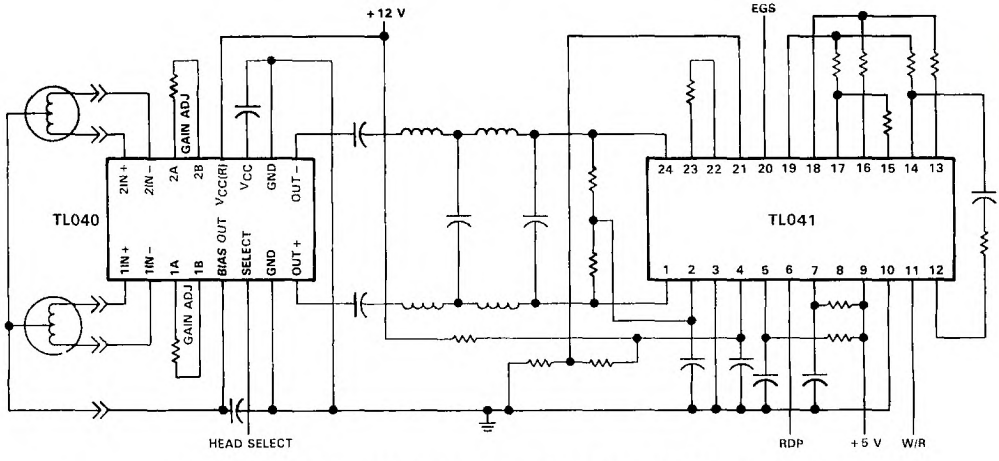
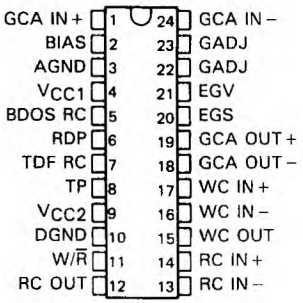


FIGURE 6. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

D3024, AUGUST 1987

- **Designed for Signal Processing in Streaming-Tape Memory Units in Combination with TL040 Two-Channel Video Amplifier**
- **Space-Saving LSI Circuits Include:**
  - **Two High-Speed Differential Comparators**
  - **Time-Domain Filter**
  - **Bidirectional One-Shot Multivibrator**
  - **Gain-Controlled Video Amplifier with Differential Inputs and Outputs**
- **Amplifier and Comparator Bandwidth . . . 20 MHz Typical**
- **Maximum Data Rate at Read Data Pulse (RDP) . . . 1.4 Mb/s Typical**
- **Available in 300-mil Dual-In-Line and "Small Outline" Plastic Packages**

DW OR NT . . . PACKAGE
(TOP VIEW)



description

The TL041 is a magnetic tape read signal conditioner designed for use with the TL040 video amplifier. When combined, these devices amplify the low-signal output from a streaming-tape playback head and reconstruct the data as originally written on the tape. The TL041C includes a gain-controlled amplifier, two comparators, read/write select logic, a time-domain filter, and a bidirectional one-shot multivibrator.

The amplifier has differential inputs, differential outputs, and electronic gain control. A special feature of the electronic gain control is the Electronic Gain Select (EGS). When the EGS input is high, the Electronic Gain Voltage (EGV) input is driven low and amplifier gain is determined by the value of the resistor connected between the Gain Adjust (GADJ) pins. When the EGS input is low, the gain set by the resistor is increased by an amount determined by the voltage applied to the EGV pin.

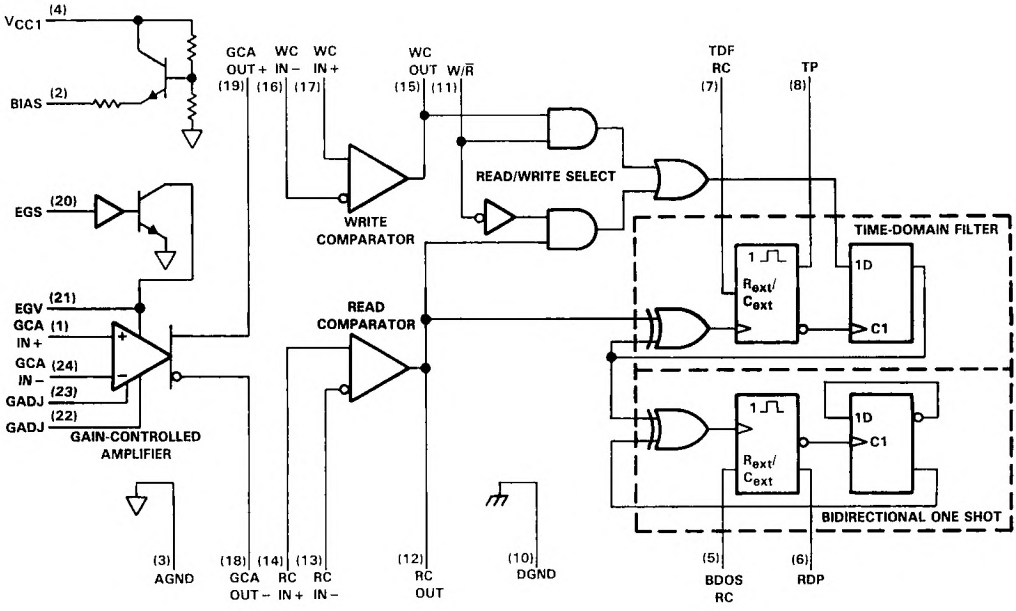
To accommodate different magnetic tape output signal levels, the amplifier gain may be switched by logic at the EGS input, controlled manually with an adjustable voltage at the EGV input, or automatically adjusted with an automatic gain control (AGC) circuit applying a control voltage to the EGV input.

The comparator functions are controlled by a logic input to the Write/Read (W/$\overline{R}$) select input. With the W/$\overline{R}$ input low, the read comparator output (usually connected as a zero-crossing detector) is sent to the time-domain filter. When W/$\overline{R}$ is high, the write comparator output is used to provide write amplitude verification in a typical read-after-write function.

The time-domain filter helps to ensure the input data is valid. A capacitor in series with a resistor, connected to the time-domain filter pin (TDF RC), begins charging at the leading edge of an input pulse from the read comparator. If the input pulse does not remain high for one RC time constant, the pulse is considered invalid and no signal is passed to the bidirectional one-shot multivibrator (BDOS). However, if the input pulse remains high for longer than one RC time constant, the pulse is considered valid and the signal is passed through the time-domain filter to trigger the BDOS. When triggered, the BDOS provides a pulse to the Read Data Pulse (RDP) output. The RDP output pulse duration is determined by a resistor-capacitor network connected to the BDOS RC pin.

The TL041C is characterized for operation from 0°C to 70°C.

functional block diagram



FUNCTION TABLE

INPUT CONDITONS			I/O NAME	I/O CONDITION
EGS	W/R̄	DIFFERENTIAL INPUTS WRITE OR READ COMPARATOR		
	X	RC IN+ > RC IN–	RC OUT	H
	X	RC IN– > RC IN+	RC OUT	L
	L	X	RC OUT	Input to time-domain filter
	X	WC IN+ > WC IN–	WC OUT	H
	X	WC IN– > WC IN+	WC OUT	L
	H	X	WC OUT	Input to time-domain filter
H		X	EGV	L
L		X	EGV	Input

TEXAS INSTRUMENTS
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PIN NAME	PIN NO.	DESCRIPTION
[illegible]	3	Analog ground
BDOS RC	5	Bidirectional one-shot resistor and capacitor
BIAS	2	Output bias voltage
DGND	10	Digital ground
EGS	20	Electronic gain select
EGV	21	Electronic gain voltage
GCA IN−	24	Gain-controlled amplifier, inverting input
GCA IN+	1	Gain-controlled amplifier, noninverting input
GADJ	22	Gain adjust
GADJ	23	Gain adjust
GCA OUT−	18	Gain-controlled amplifier, inverting output
GCA OUT+	19	Gain-controlled amplifier, noninverting output
RC IN−	13	Read comparator, inverting input
RC IN+	14	Read comparator, noninverting input
RC OUT	12	Read comparator out
RDP	6	Read data pulse
TDF RC	7	Time-domain filter resistor and capacitor
TP	8	Test point
V_{CC1}	4	Analog collector supply voltage
V_{CC2}	9	Digital collector supply voltage
WC IN−	16	Write comparator, inverting input
WC IN+	17	Write comparator, noninverting input
WC OUT	15	Write comparator out
W/$\overline{R}$	11	Write/read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage: V_{CC1} (see Note 1) . . . . . 14 V
V_{CC2} . . . . . 7 V
Input voltage range: Amplifier and comparators . . . . . AGND − 0.2 V to V_{CC1} + 0.2 V
Multivibrators and logic . . . . . AGND − 0.2 V to V_{CC2} + 0.2 V
Input current: EGV (see Note 2) . . . . . ±2 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltages except differential voltages are with respect to network ground terminals (AGND and DGND tied together).
2. Driving EGV high from a low-impedance source (> ±2 mA capability) with EGS high can result in damage to the device.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	[illegible] mW	10.8 mW/°C	[illegible]
NT	1700 mW	13.6 mW/°C	1088 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		[illegible]	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
High-level input voltage, V_{IH}	EGS or W/$\overline{R}$	2			V
Low-level input voltage, V_{IL}	EGS or W/$\overline{R}$			0.8	V
Input voltage, V_I	[illegible]	0		10	V
	[illegible]	0		$0.8V_{CC1}$	
Common-mode input voltage to gain-control amplifier, V_{IC}			4		V
High-level output current, I_{OH}	WC OUT, RC OUT, TP, or RDP			−400	μA
Low-level output current, I_{OL}	WC OUT, RC OUT, TP, or RDP			8	mA
Pulse duration, t_w	TP or [illegible]	40			ns
External timing resistance, (see Note 3)	TDF or BDOS RC	5		25	kΩ
External timing capacitance	TDF or BDOS RC)	0.01	0.1	1000	nF
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Some high resistance and capacitance combinations may produce abnormal output waveforms.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at V_{CC1} = 12 V, V_{CC2} = 5 V, $V_{IC(GIC)}$ = V_{bias}, R_{ADJ} = 5 kΩ, EGS at high level, EGV at 0 V, r_i = 50 Ω, R_L = 2 kΩ, T_A = 25°C (unless otherwise noted)

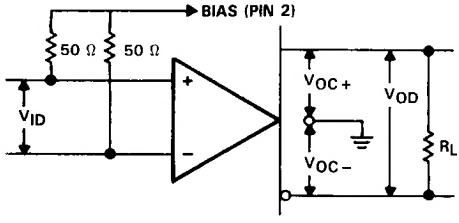
gain-controlled amplifier

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	1	V_{ID} = 0,	V_{OD} = V_O		0.35	0.75	V
V_{OPP}	Maximum differential output voltage	1	V_{ID} = 1 V,	V_{OPP} = V_O	3	4		V
A_{VD}	Large-signal differential voltage amplification	1	V_{ID} = 20 mV,	EGV high	8	14	20	V/V
			V_{id} = 20 mV, EGS low, f = 455 kHz	EGV at 4 V		19		V/V
				EGV at 9.6 V		90		
CMRR	Common-mode rejection ratio	2	V_{IC} = 2 V to 5 V		60	80		dB
V_{IC}	Common-mode input voltage	2			2		5	V
V_{OC}	Common-mode output voltage	1	V_{ID} = 0		4	5	6	V
I_{IO}	Input offset current	1	$I_{IB+} - I_{IB-}$			0.2	3	μA
I_O	Output current, sink				1.5	2		mA
I_{IB}	Input bias current	1	$(I_{IB+} + I_{IB-})/2$			5	17	μA
$V_{O(BIAS)}$	Bias output voltage	1			3	4	5	V
$z_{o(BIAS)}$	Bias output impedance					1		kΩ
z_i	Input impedance					30		kΩ
BW	Bandwidth (−3 dB)	3				20		MHz
k_{SVR}	Supply voltage rejection ratio	4	V_{CC1} = 10.8 V to 13.2 V		50	70		dB
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	No signal		32	45	mA

logic section

PARAMETER			TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage			V_{CC2} = 4.5 V, I_{OH} = −400 μA	V_{ID} = 0.1 V,	2.7	3.5		V
V_{OL}	Low-level output voltage			V_{CC2} = 4.5 V, I_{OL} = 8 mA	V_{ID} = 0.1 V,		260	500	mV
V_{ICR}	Common-mode input voltage, comparators					2		7	V
I_{IH}	High-level input current	EGS		$V_{I(EGS)}$ = 2.7 V			120	200	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 2.7 V				20	
I_{IL}	Low-level input current	EGS		$V_{I(EGS)}$ = 0.4 V				−20	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 0.4 V				−400	
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 5.5 V,	No signal		22	31	mA
	Response time			100-mV step,	5-mV overdrive		50		ns
t_w	Pulse duration of one-shots (TP, RDP)			R_{ext} = 5 kΩ,	C_{ext} = 1 nF		360		ns
				R_{ext} = 20 kΩ,	C_{ext} = 33 pF		460		

PARAMETER MEASUREMENT INFORMATION



$V_{OO} = V_{OD}$ with $V_{ID} = 0$

$V_{OPP} = V_{OD}$ with $V_{ID} = 1$ V

$A_{VD} = \frac{V_{OD}}{V_{ID}}$ with $V_{ID} = 20$ mV

$V_{OC} = \frac{V_{OC+} + V_{OC-}}{2}$ with $V_{ID} = 0$

FIGURE 1

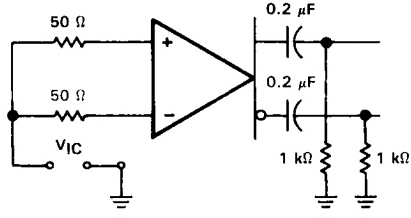


FIGURE 2

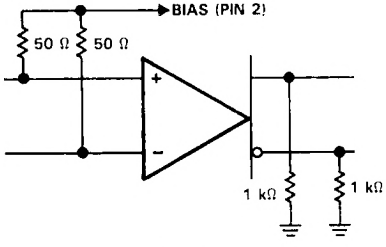


FIGURE 3

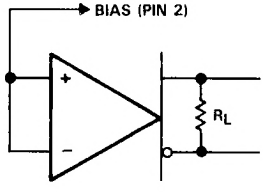


FIGURE 4

4 Special Functions

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TYPICAL CHARACTERISTICS

READ DATA PULSE DURATION
vs
CAPACITANCE

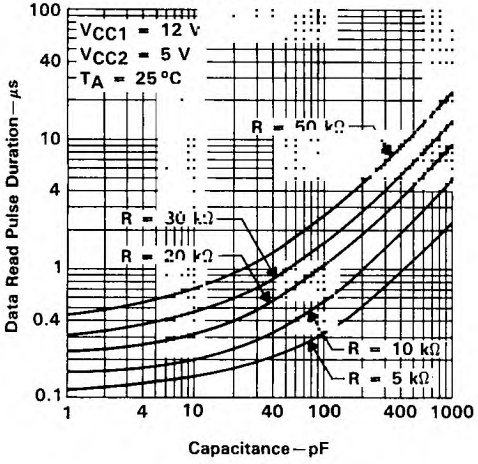


FIGURE 5

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
ELECTRONIC GAIN VOLTAGE

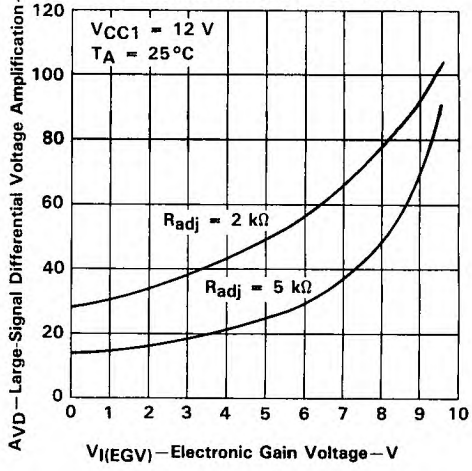


FIGURE 6

TYPICAL APPLICATION DATA

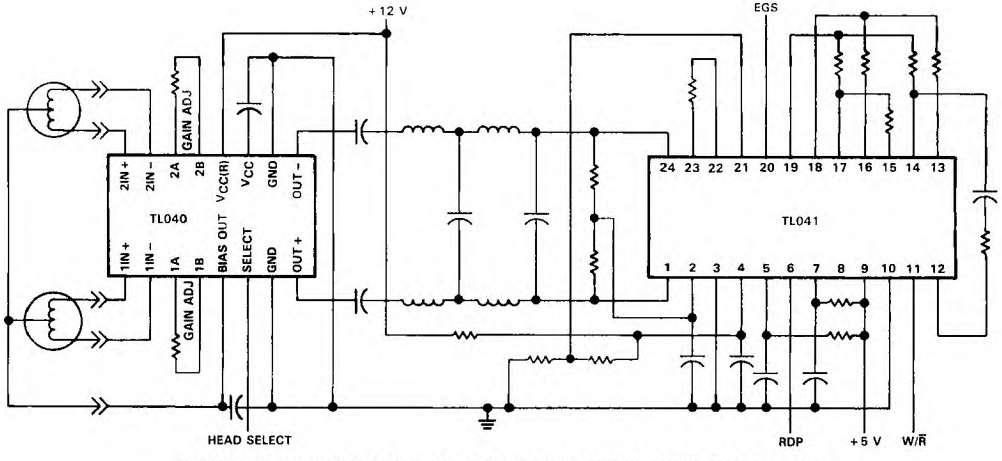
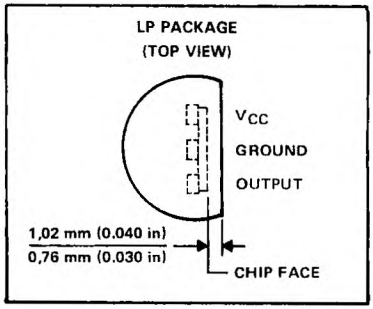


FIGURE 7. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

4
Special Functions

D2408, DECEMBER 1977, REVISED APRIL 1988

- Magnetic-Field Sensing Hall-Effect Input
- On-Off Hysteresis
- Small Size
- Solid-State Technology
- Open-Collector Output



description

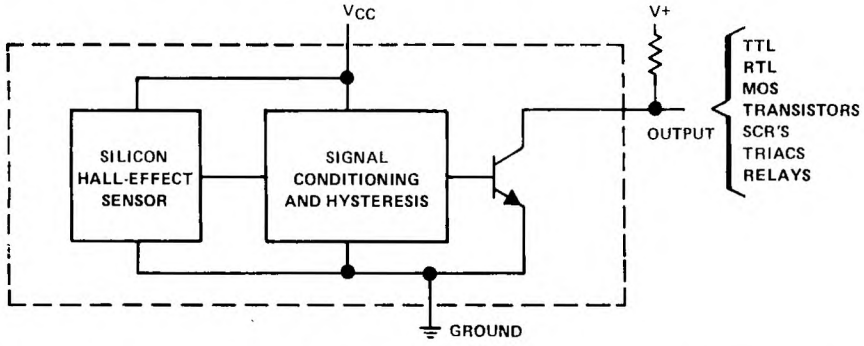
The TL170C is a low-cost magnetically operated electronic switch that utilizes the Hall Effect to sense steady-state magnetic fields. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

The TL170C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE (T_A = 25°C)

FLUX DENSITY	OUTPUT
≤ −25 mT	Off
−25 mT < B < 25 mT	Undefined
≥ 25 mT	On

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Output voltage . . . . . 30 V
Output current . . . . . 20 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Magnetic flux density . . . . . unlimited

NOTE 1. Voltage values are with respect to network ground terminal.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V ± 5% (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
B_{T+}	Threshold of positive-going magnetic flux density†			25°C			25	mT‡
				0°C to 70°C			35	
B_{T-}	Threshold of negative-going magnetic flux density†			25°C	−25§			mT‡
				0°C to 70°C				
$B_{T+} - B_{T-}$	Hysteresis			0°C to 70°C		20		mT‡
I_{OH}	High-level output current	V_{OH} = 20 V		0°C to 70°C			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 16 mA		0°C to 70°C			0.4	V
I_{CC}	Supply current	V_{CC} = 5.25 V	Output low	0°C to 70°C			6	mA
			Output high				4	

†Threshold values are those levels of magnetic flux denisity at which the output changes state. For the TL170C, a level more positive than B_{T+} causes the output to go to a low level and a level more negative than B_{T-} causes the output to go to a high level. See Figures 1 and 2.

‡The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten.

§The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for flux-density threshold levels only.

The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

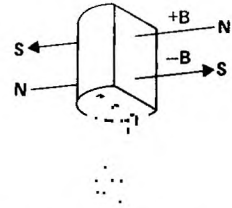
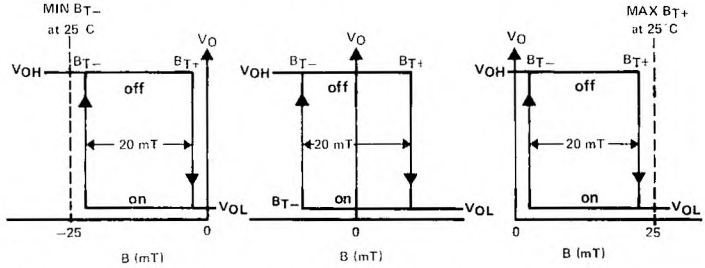


FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY



The positive-going threshold (B_{T+}) may be a negative or positive B level at which a positive-going (decreasing negative or increasing positive) flux density results in the TL170 output turn-on. The negative-going threshold is a positive or negative B level at which a negative-going (decreasing positive or increasing negative) flux density results in the TL170 turning off.

FIGURE 2. REPRESENTATIVE CURVES OF V_O vs B

TEXAS INSTRUMENTS
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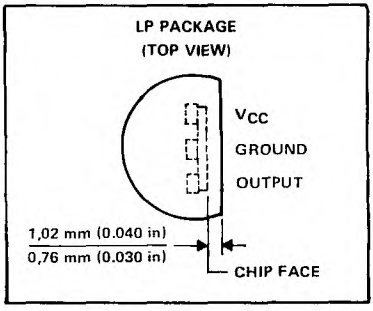
D2490, AUGUST 1977—REVISED APRIL 1988

- Magnetic-Field Sensing Hall-Effect Input
- On-Off Hysteresis
- Small Size
- Solid-State Technology
- Open-Collector Output
- Normally Off Switch



description

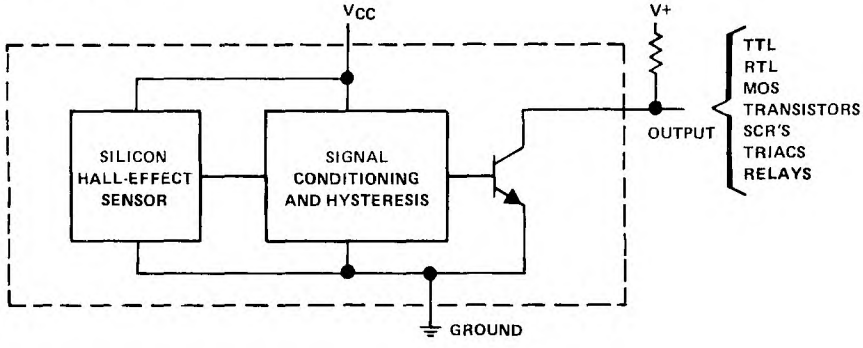
The TL172C is a low-cost magnetically operated normally off electronic switch that utilizes the Hall Effect to sense the presence of a magnetic field. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. A magnetic field of sufficient strength in the positive direction will cause the TL172C output to be in a low-impedance state. Otherwise, the output will present a high impedance. The output of this circuitry connected to many different types of electronic components.

The TL172C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE

FLUX DENSITY	OUTPUT
≤ 10 mT	Off
10 mT < B < 60 mT	Undefined
≥ 60 mT	On

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

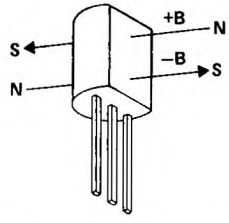
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Output voltage . . . . . 30 V
Output current . . . . . 20 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Magnetic flux density . . . . . unlimited

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over rated operating free-air temperature range, V_{CC} = 5 V ± 5% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{T+}	Threshold of positive-going magnetic flux density†				60	mT‡
B_{T-}	Threshold of negative-going magnetic flux density†		10			mT‡
$B_{T+} - B_{T-}$	Hysteresis			23		mT‡
I_{OH}	High-level output current	V_{OH} = 20 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 16 mA			0.4	V
I_{CC}	Supply current	V_{CC} = 5.25 V			6	mA

†Threshold values are those levels of magnetic flux density at which the output changes state. For the TL172C, a level more positive than B_{T+} causes the output to go to a low level, and a level more negative than B_{T-} causes the output to go to a high level. See Figures 1 and 2.
‡The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux amanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY

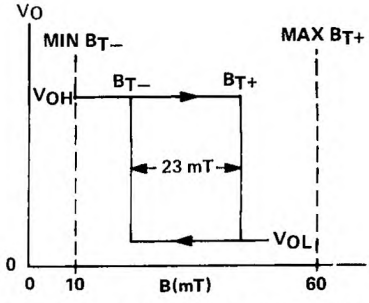
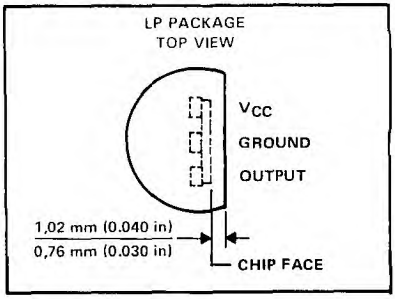


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2526, MARCH 1979—REVISED APRIL 1988

- **Output Voltage Linear with Applied Magnetic Field**
- **Sensitivity Constant Over Wide Operating Temperature Range**
- **Solid-State Technology**
- **Three-Terminal Device**
- **Senses Static or Dynamic Magnetic Fields**

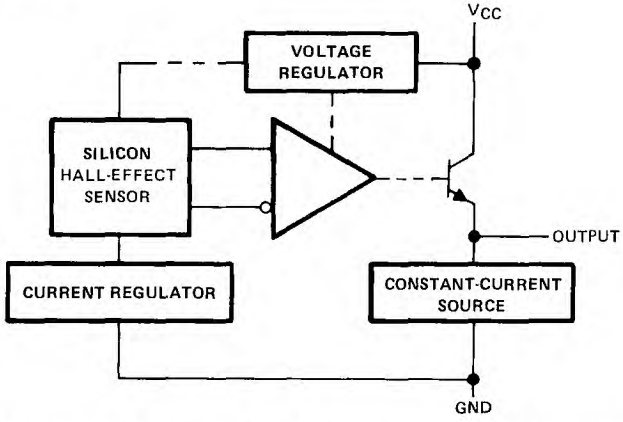


description

The TL173I and TL173C are low-cost magnetic-field sensors designed to provide a linear output voltage proportional to the magnetic field they sense. These monolothic circuits incorporate a Hall element as the primary sensor along with a voltage reference and a precision amplifier. Temperature stabilization and internal trimming circuitry yield a device that features high overall sensitivity accuracy with less then 5% error over its operating temperature range.

The TL173I is characterized for operation from −20°C to 85°C. The TL173C is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	775 mW
Operating free-air temperature range: TL173I	−20°C to 85°C
TL173C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Magnetic flux densisty	unlimited

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C.

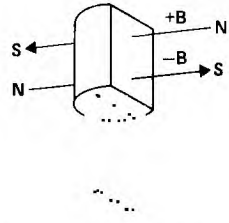
recommended operating conditions

		TL173I			TL173C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		10.8	12	13.2	10.8	12	13.2	V
Magnetic flux density, B				±50			±50	mT
Output current, I_O	Sink			0.5			0.5	mA
	Source			−2			−2	
Operating free-air temperature, T_A		−20		85	0		70	°C

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_O	Output voltage	I_O = −2 mA to 0.5 mA,		5.8	6	6.2	V
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	B = 0 mT§,	T_A = 25°C		18		mV/V
S	Magnetic sensitivity ($\Delta V_O/\Delta B$)	B = −50 to 50 mT§,	T_A = 25°C	13.5	15	18	V/T§
ΔS	Magnetic sensitivity change with temperature	ΔT_A = 25°C to MIN or MAX				±5	%
I_{CC}	Supply current	B = 0 mT§,	I_O = 0		8	12	mA
f_{max}	Maximum operating frequency				100		kHz

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Typical values are at V_{CC} = 12 V and T_A = 25°C.
§ The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten, e.g., 50 millitesla = 500 gauss.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY

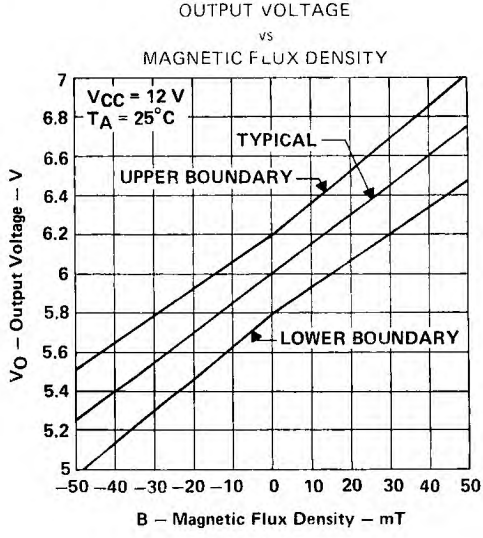


FIGURE 2

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

The circuit in Figure 3 may be used to set the output voltage at zero field strength to exactly 6 V (using R1), and to set the sensitivity to exactly −15 V/T (using R2), as depicted in Figure 4.

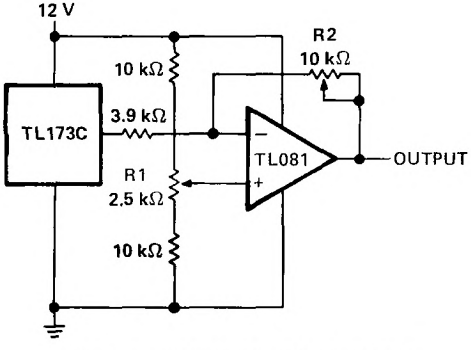


FIGURE 3. COMPENSATION CIRCUIT

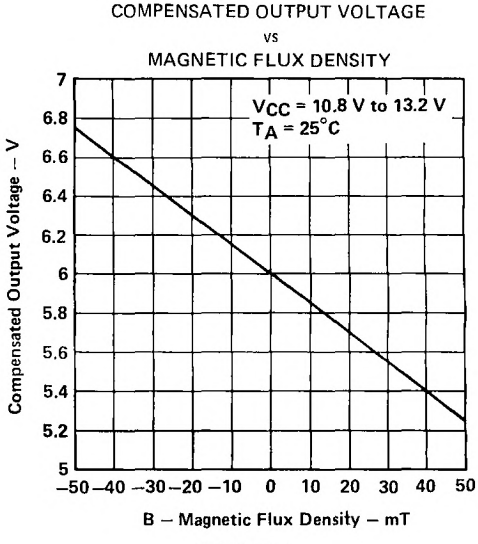


FIGURE 4

D956, JUNE 1976—REVISED FEBRUARY 1989

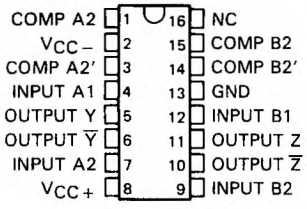
- **Excellent Dynamic Range**
- **Wide Bandwidth**
- **Built-In Temperature Compensation**
- **Log Linearity (30 dB Sections) . . . 1 dB Typ**
- **Wide Input Voltage Range**

description

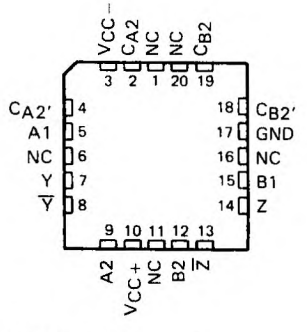
This monolithic amplifier circuit contains four 30-dB logarithmic stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dB input voltage range. Each half of the circuit contains two of these 30-dB stages summed together in one differential output that is proportional to the sum of the logarithms of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120 dB. In practice, this permits the input voltage range to be typically greater than 80 dB with log linearity of ± 0.5 dB (see application data). Bandwidth is from dc to 40 MHz.

This circuit is useful in military weapons systems, broadband radar, and infrared reconnaissance systems. It serves for data compression and analog compensation. This logarithmic amplifier is used in log IF circuitry as well as video and log amplifiers. The TL441AM is characterized for operation over the full military temperature range of −55°C to 125°C.

J PACKAGE
(TOP VIEW)

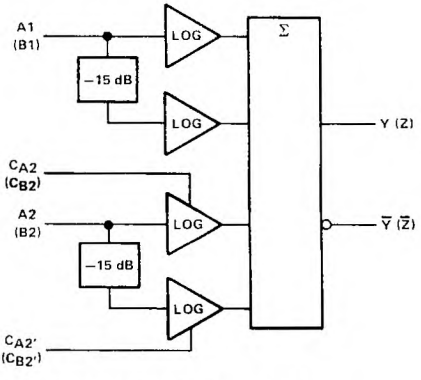


FK PACKAGE
(TOP VIEW)



NC—No internal connection

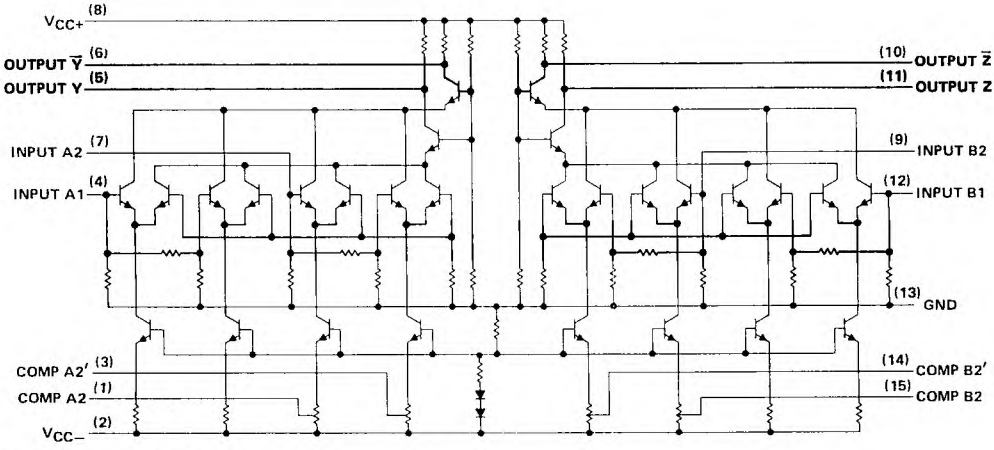
functional block diagram (one half)



$Y \propto \log A1 + \log A2$; $Z \propto \log B1 + \log B2$
where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.
C_{A2}, $C_{A2'}$, C_{B2}, and $C_{B2'}$ are detector compensation inputs.

4 Special Functions

schematic



Pin numbers shown are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1): V_{CC+} . . . . . 8 V
V_{CC-} . . . . . −8 V
Input voltage (see Note 1) . . . . . 6 V
Output sink current (any one output) . . . . . 30 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE: 1. All voltages, except differential output voltages, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	500 mW	11.0 mW/°C	104°C	500 mW	275 mW
J	500 mW	11.0 mW/°C	104°C	500 mW	275 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Peak-to-peak input voltage for each 30-dB stage	0.01		1	V
Operating free-air temperature, T_A	−55		125	°C

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electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST FIGURE	MIN	TYP	MAX	UNIT
Differential output offset voltage	1		±25	±70	mV
Quiescent output voltage	2	5.45	5.6	5.85	V
DC scale factor (differential output), each 3-dB stage, −35 dBV to −5 dBV	3	7	8	11	mV/dB
AC scale factor (differential output)			8		mV/dB
DC error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	3		1	2.6	dB
Input impedance			500		Ω
Output impedance			200		Ω
Rise time, 10% to 90% points, C_L = 24 pF	4		20	35	ns
Supply current from V_{CC+}	2	14.5	18.5	23	mA
Supply current from V_{CC-}	2	−6	−8.5	−11	mA
Power dissipation	2	123	162	207	mW

electrical characteristics over operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	MIN	TYP	MAX	UNIT
Differential output offset voltage		1			±100	mV
Quiescent output voltage		2	5.3		5.85	V
DC scale factor (differential output) each 30-dB stage, −35 dBV to −5 dBV		3	7		11	mV/dB
DC error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	T_A = −55°C	3			4	dB
	T_A = 125°C				3	
Supply current from V_{CC+}		2	10		31	mA
Supply current from V_{CC-}		2	−4.5		−15	mA
Power dissipation		2	87		276	mW

PARAMETER MEASUREMENT INFORMATION

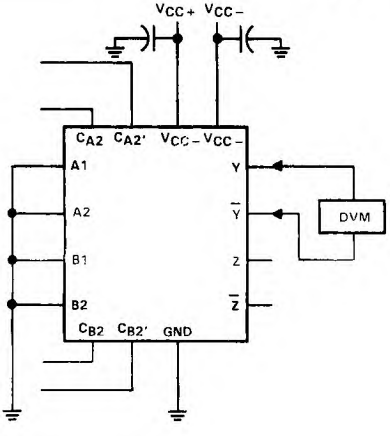


FIGURE 1

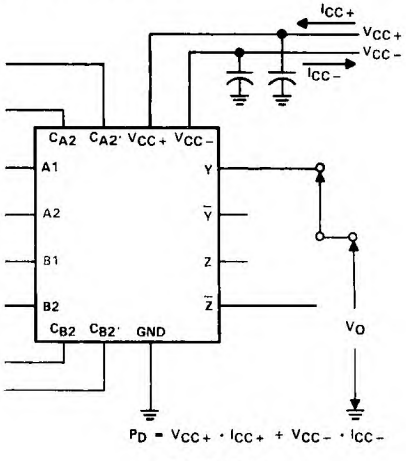
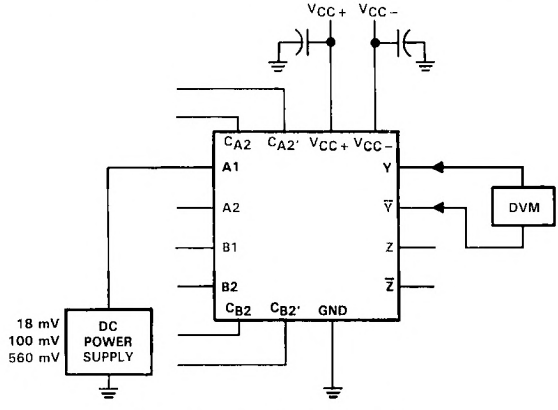


FIGURE 2

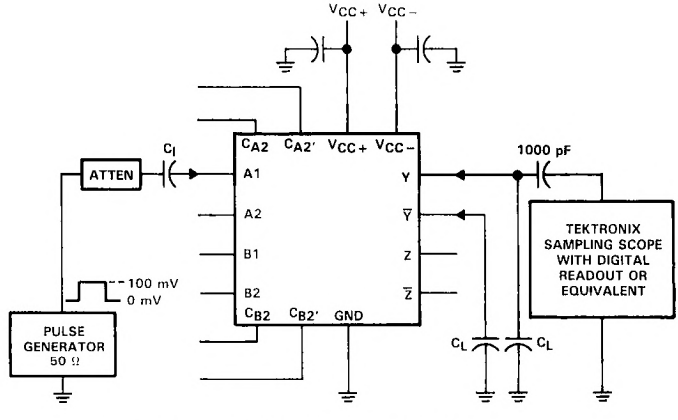
PARAMETER MEASUREMENT INFORMATION



$$\text{Scale Factor} = \frac{|V_{out(560\ mV)} - V_{out(18\ mV)}|\ mV}{30\ dB}$$

$$\text{Error} = \frac{|V_{out(100\ mV)} - 0.5\ V_{out(560\ mV)} - 0.5\ V_{out(18\ mV)}|}{\text{Scale Factor}}$$

FIGURE 3



NOTES: A. The input pulse has the following characteristics: t_w = 200 ns, $t_r \leq 2$ ns, $t_f \leq 2$ ns, PRR ≤ 10 MHz.
B. Capacitor C_I consists of three capacitors in parallel: 1 μF, 0.1 μF, and 0.01 μF.
C. C_L includes probe and jig capacitance.

FIGURE 4

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TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

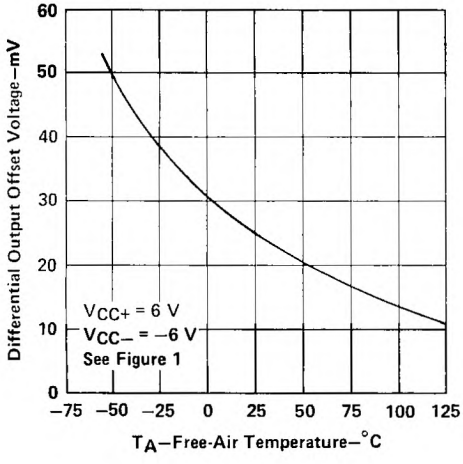

FIGURE 5

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

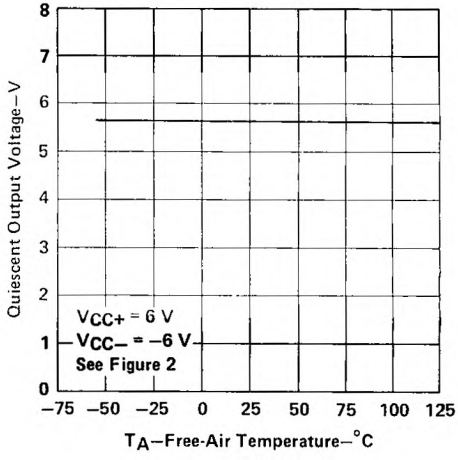

FIGURE 6

DC SCALE FACTOR
vs
FREE-AIR TEMPERATURE

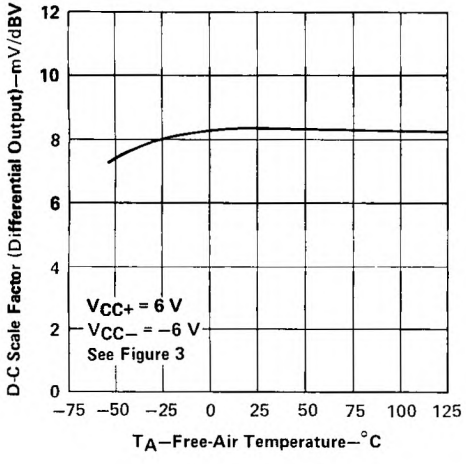

FIGURE 7

DC ERROR
vs
FREE-AIR TEMPERATURE

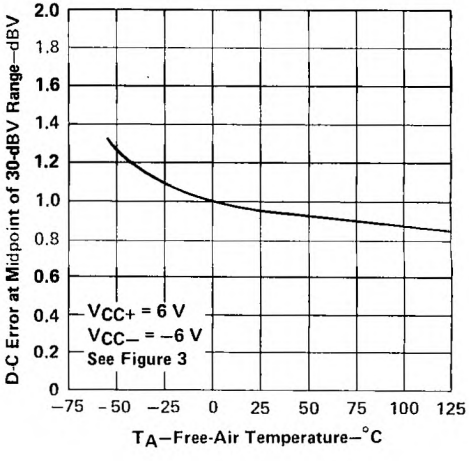

FIGURE 8

TYPICAL CHARACTERISTICS

OUTPUT RISE TIME
vs
LOAD CAPACITANCE

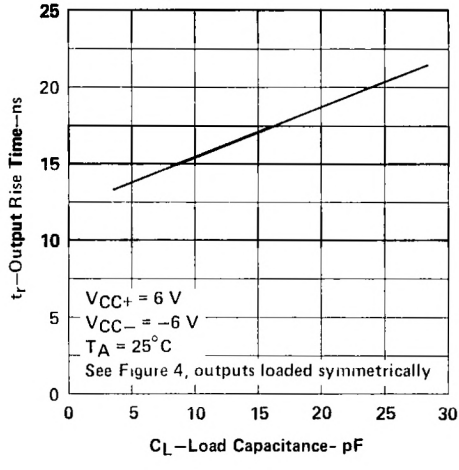

FIGURE 9

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

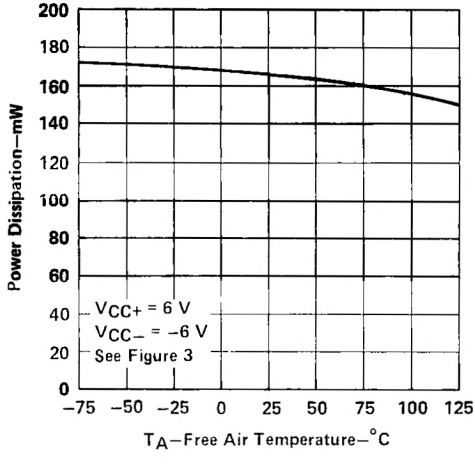

FIGURE 10

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TYPICAL APPLICATION DATA

Although designed for high-performance applications such as broadband radar infrared detection and weapons systems, this device has a wide range of applications in data compression and analog computation.

basic logarithmic function

The basic logarithmic response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln [(I_C + I_{CES})/I_{CES}]$$

where:

I_C = collector current
I_{CES} = collector current at $V_{BE} = 0$
$m = q/kT$ (in V^{-1})
V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to common-mode noise.

functional block diagram

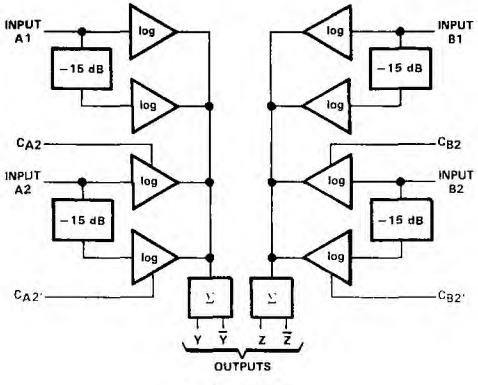


FIGURE 11

logarithmic sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dB log subsection, and each input feeds two pairs for a range of 30-dB per stage.

Four compensation points are made available to allow slight variations in the gain (slope) of the two individual 15-dB stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from its quiescent value, the gain of that particular 15-dB stage can be adjusted to match the other 15-dB stage in the pair. The compensation pins may also be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\overline{Y}$ (or Z and $\overline{Z}$) which are equal in amplitude but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, linear attentuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 V to 1 V. Input levels in excess of 1 V may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that may be applied. As the input drive reaches ±3.5 V, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ±3 V to ensure a clean output.

output levels

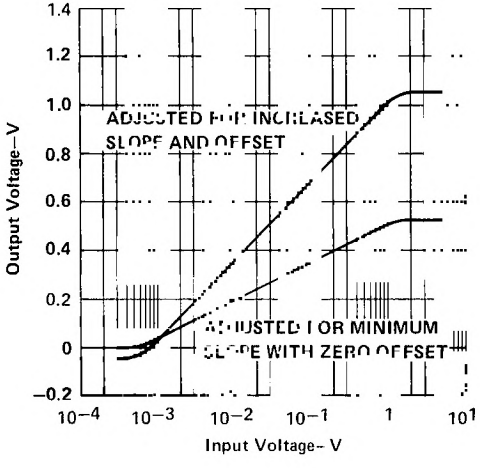
Differential-output-voltage levels are low, generally less than 0.6 V. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin may also be adjusted by positioning the offset of the output buffer.

TYPICAL APPLICATION DATA

circuits

Figures 12 through 19 show typical circuits using this logarithmic amplifier. Operational amplifiers not otherwise designated are TLC271. For operation at higher frequencies, the TL592 is recommended instead of the TLC271.

TYPICAL TRANSFER CHARACTERISTICS



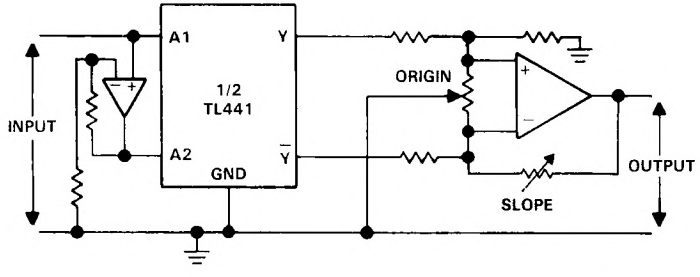


FIGURE 12. OUTPUT SLOPE AND ORIGIN ADJUSTMENT

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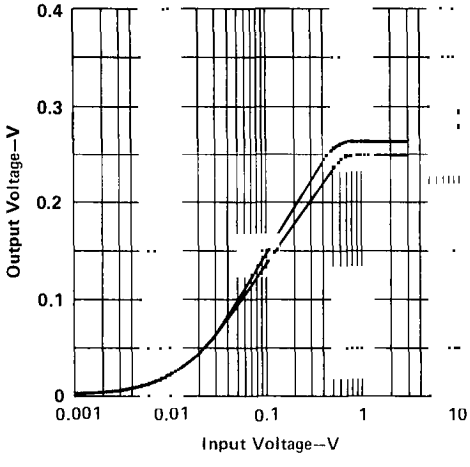
TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS
OF TWO TYPICAL INPUT STAGES



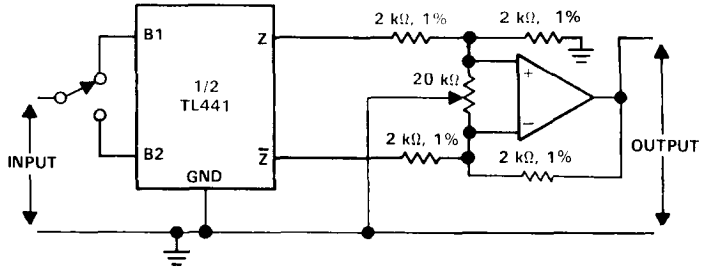
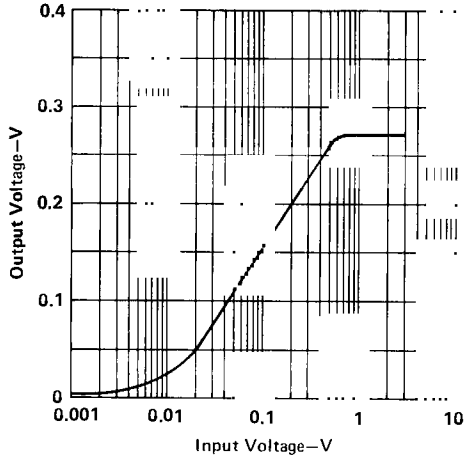


FIGURE 13. UTILIZATION OF SEPARATE STAGES

TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS
WITH BOTH SIDES PARALLELED



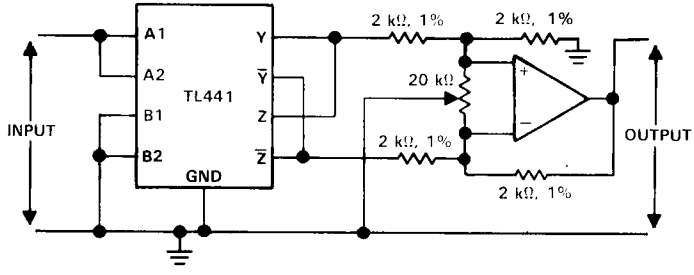


FIGURE 14. UTILIZATION OF PARALLELED INPUTS

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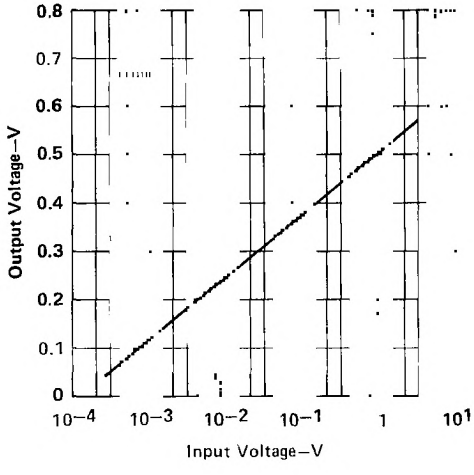
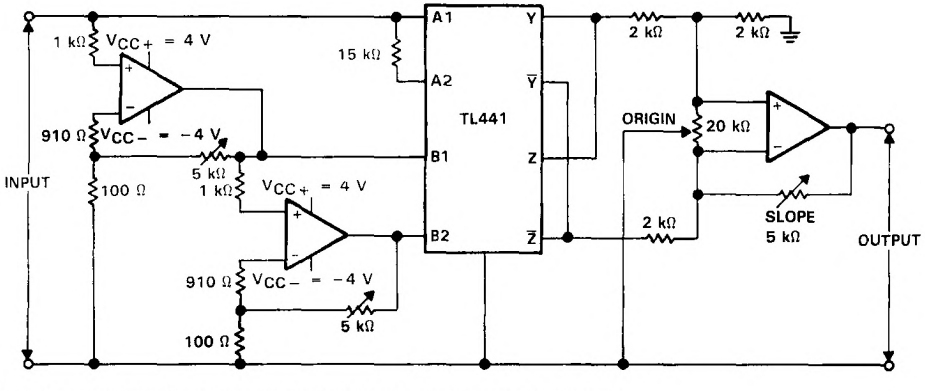
TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS

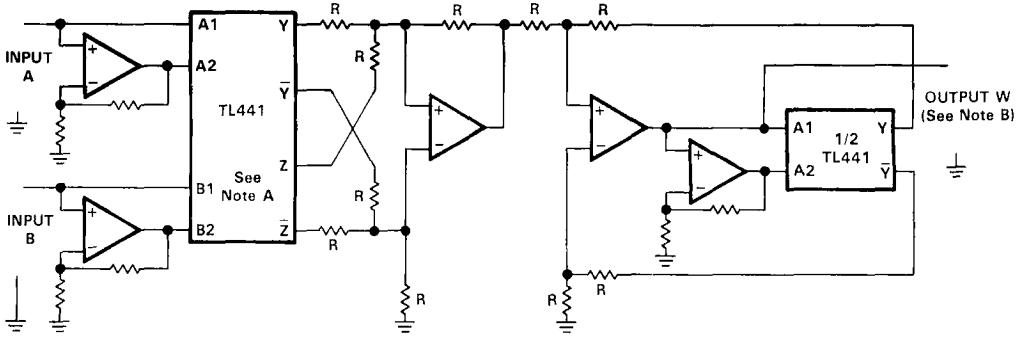




NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ±4 V.
B. The gains of the input amplifiers are adjusted to achieve smooth transistions.

Figure 15. LOGARITHMIC AMPLIFIER WITH INPUT VOLTAGE RANGE GREATER THAN 80 dB

TYPICAL APPLICATION DATA

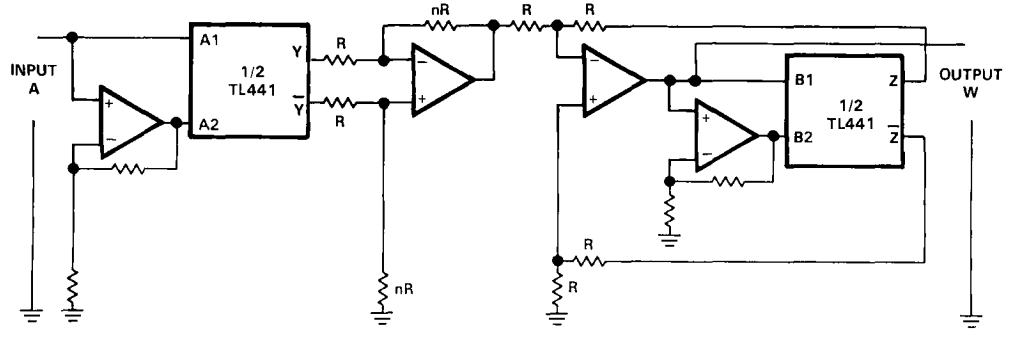


NOTES: A. Connections shown are for multiplication. For division, Z and $\overline{Z}$ connections are reversed.
B. Output W may need to be amplified to give actual product or quotient of A and B.
C. R designates resistors of equal value, typically 2 kΩ to 10 kΩ.

Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$

Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A + \log_a B)}$

FIGURE 16. MULTIPLICATION OR DIVISION



NOTE: R designates resistors of equal value, typically 2 kΩ to 10 kΩ. The power to which the input variable is raised is fixed by setting nR. Output W may need to be amplified to give the correct value.

Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

FIGURE 17. RAISING A VARIABLE TO A FIXED POWER

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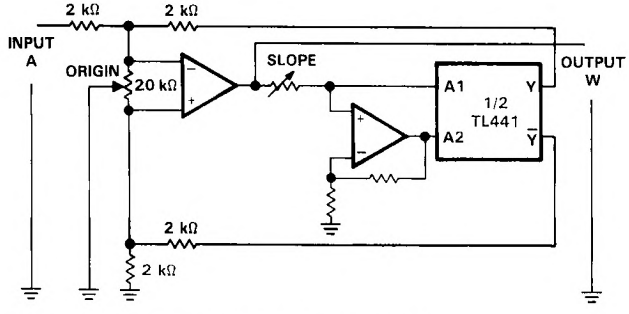
TYPICAL APPLICATION DATA



NOTE: Adjust the slope to correspond to the base "a".
Exponential to any base: W = a

FIGURE 18. RAISING A FIXED NUMBER TO A VARIABLE POWER

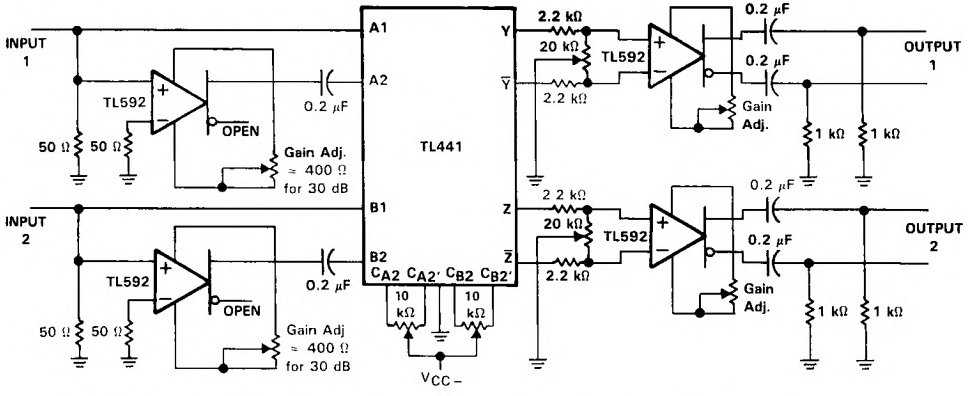
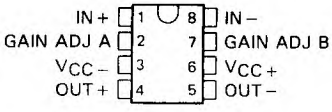


FIGURE 19. DUAL-CHANNEL RF LOGARITHMIC AMPLIFIER WITH 50-dB INPUT RANGE PER CHANNEL AT 10 MHz

D2668, NOVEMBER 1983–REVISED MAY 1988

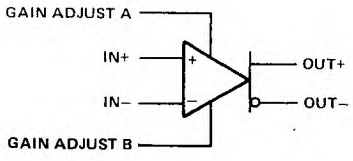
- **8-Pin Version of NE592 . . . Saves Printed Circuit Board Space**
- **Adjustable Gain to 400**
- **No Frequency Compensation Required**
- **Adjustable Passband**

D OR P PACKAGE
(TOP VIEW)



DEVICE TYPE	TEMPERATURE RANGE	A_{VD} RANGE (GAIN OPTION 1)
TL592	0°C to 70°C	250–600
TL592A	0°C to 70°C	400–600

symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs.

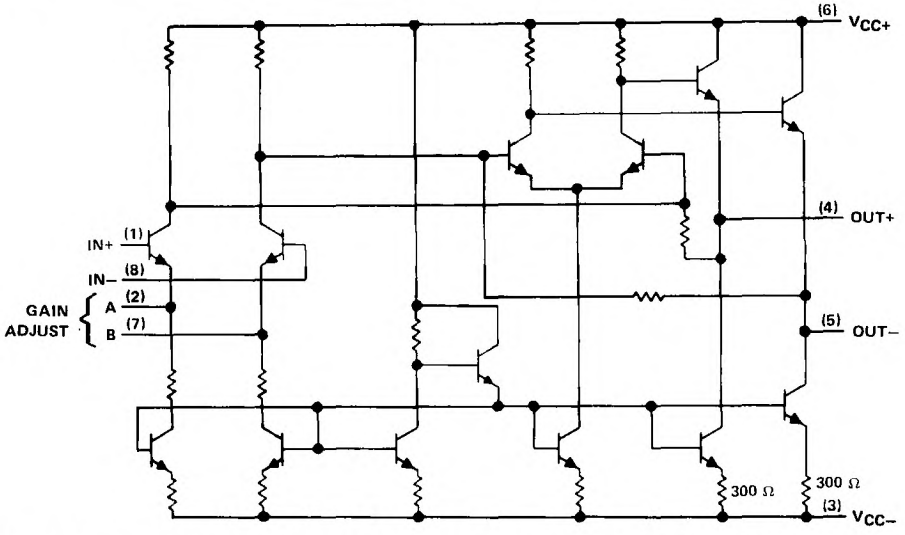
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of nominally 400 may be selected without external components, or amplification may be adjusted from 0 to approximately 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The TL592 and TL592A are characterized for operation from 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation at 70°C . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics at specified free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		GAIN OPTION†	TL592			TL592A			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	25°C	1	250	400	600	400	440		V/V
				0°C to 70°C		250		600	400			
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	25°C	1		50			50		MHz
I_{IO}	Input offset current		V_{IC} = 0	25°C	1 or 2		0.4	5		0.4	5	μA
				0°C to 70°C				6			6	
I_{IB}	Input bias current		V_{IC} = 0	25°C	1 or 2		9	30		10	30	μA
				0°C to 70°C				40			40	
V_{ICR}	Common-mode input voltage range	3		25°C	1 or 2	±1			±1			V
				0°C to 70°C		±1			±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞	25°C	2	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	25°C	2		0.35	0.75		0.35	0.75	V
				0°C to 70°C				1.5			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	R_L = 2 kΩ	25°C	1	3	4		3	4		V
				0°C to 70°C		2.8			2.8			
z_i	Input impedance		V_{OD} = 1 V, f = 1 kHz to 10 MHz	25°C	1		4			3.6		kΩ
				0°C to 70°C			3.6			3.3		
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 Hz	25°C	1	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz				60			60		
			V_{IC} = ±1 V, f = 100 kHz	0°C to 70°C		50			50			
			V_{IC} = ±1 V, f = 5 MHz				60			60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	25°C	1	50	70		50	70		dB
				0°C to 70°C		50			50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	25°C	1 or 2		12			12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	25°C	2		7.5			7.5		ns
t_r	Rise time	2	ΔV_O = 1 V	25°C	2		10.5			10.5		ns
$I_{sink(max)}$	Maximum output sink current				1, 2, or 3	3	4		3	4		mA
I_{CC}	Supply current		No load, No signal	25°C	1 or 2		18	24		19	24	mA
				0°C to 70°C				27			27	

†The gain option is selected as follows:
Gain Option 1 . . . Gain adjust pin A is connected to pin B.
Gain Option 2 . . . Gain adjust pins A and B are open.

PARAMETER MEASUREMENT INFORMATION

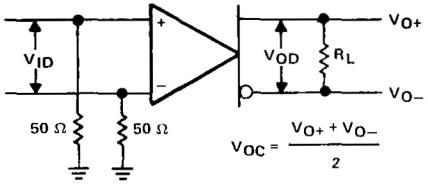


FIGURE 1

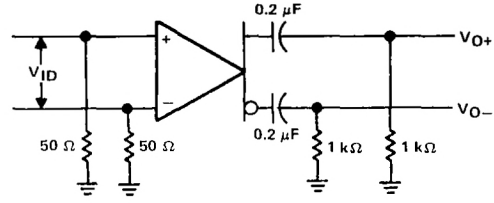


FIGURE 2

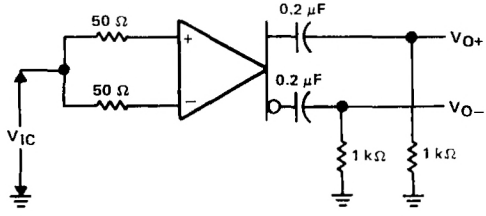


FIGURE 3

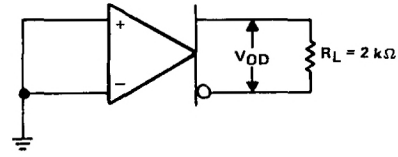


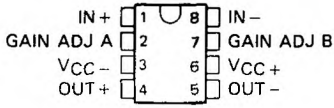
FIGURE 4

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

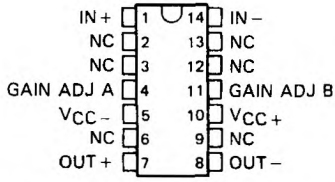
D2668, JUNE 1985—REVISED APRIL 1988

- Adjustable Gain to 400 Typ
- No Frequency Compensation Required
- Low Noise . . . 3 μV Typ V_n

D8† OR P PACKAGE
(TOP VIEW)



D14† OR N PACKAGE
(TOP VIEW)



NC—No internal connection

†D8 and D14 are the codes used to differentiate the 8-pin and 14-pin versions, respectively.

description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

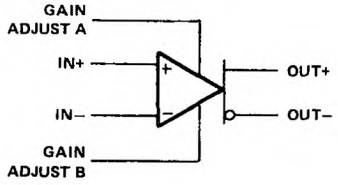
The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted from near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

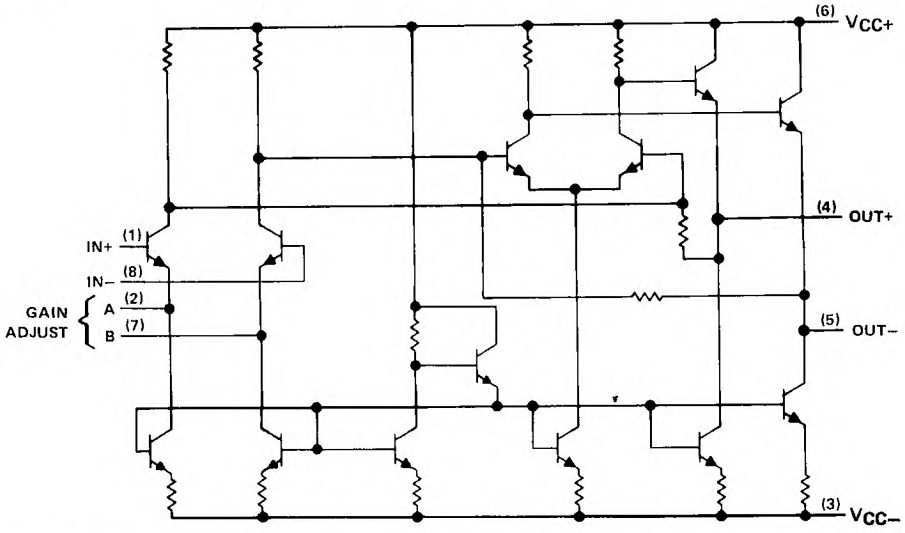
The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

symbol



schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} . . . . . −8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D8	mW	5.8 mW/°C	59°C	464 mW
D14	530 mW	N/A	N/A	530 mW
N	530 mW	N/A	N/A	530 mW
P	530 mW	N/A	N/A	530 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}			8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 0	R_L = 2 kΩ,	25°C	300	400	500	V/V
					0°C to 70°C			600	
A_{VD2}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 1 kΩ	R_L = 2 kΩ,	25°C		13		V/V
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V,	R_{AB} = 0	25°C		50		MHz
I_{IO}	Input offset current				25°C		0.4	5	μA
					0°C to 70°C			6	
I_{IB}	Input bias current				25°C		9	30	μA
					0°C to 70°C			40	
V_{ICR}	Common-mode input voltage range	3			25°C	±1			V
					0°C to 70°C	±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞		25°C	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_{AB} = ∞, R_L = ∞		25°C		0.35	0.75	V
					0°C to 70°C			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	R_L = 2 kΩ	R_{AB} = 0	25°C	3	4		V
					0°C to 70°C	2.8			
r_i	Input resistance		V_{OD} = 1 V,	R_{AB} = 0	25°C		4		kΩ
					0°C to 70°C		3.6		
r_o	Output resistance				0°C to 70°C			30	Ω
C_i	Input capacitance				25°C		5		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, R_{AB} = 0	f = 100 kHz	25°C	60	86		dB
				f = 5 MHz			60		
				f = 100 kHz	0°C to 70°C	50			
				f = 5 MHz			60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V, R_{AB} = 0		25°C	50	70		dB
					0°C to 70°C	50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C		3		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		25°C		7.5		ns
t_r	Rise time	2	ΔV_O = 1 V		25°C		10.5		ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V,	V_O = 3 V		3	4		mA
I_{CC}	Supply current		No load,	No signal	25°C		18	24	mA
					0°C to 70°C			27	

†R_{AB} is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.

PARAMETER MEASUREMENT INFORMATION

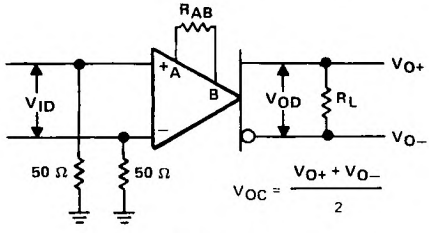


FIGURE 1

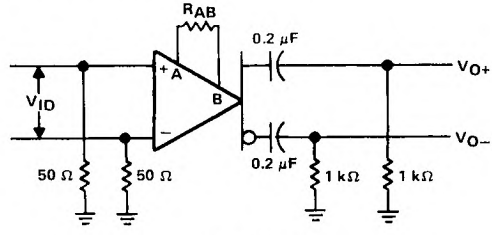


FIGURE 2

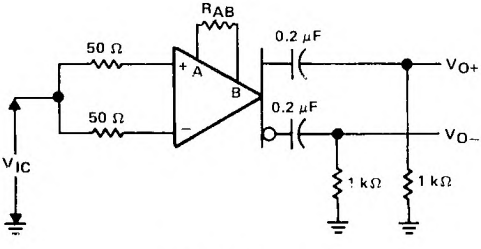


FIGURE 3

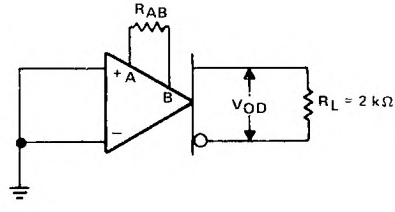


FIGURE 4

TYPICAL CHARACTERISTICS

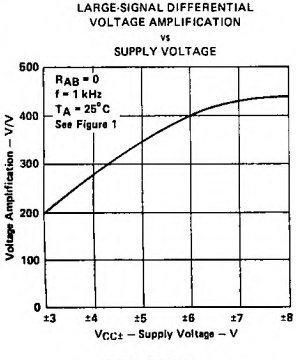


FIGURE 5

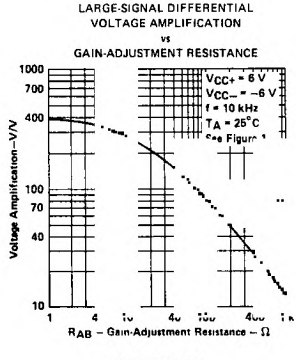


FIGURE 6

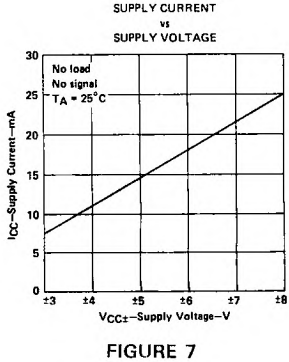


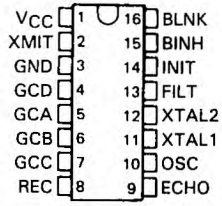
FIGURE 7

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2760, SEPTEMBER 1983—REVISED MARCH 1988

- **Designed for Use with the TL852 in Sonar Ranging Modules Like the SN28827**
- **Operates with Single Supply**
- **Accurate Clock Output for External Use**
- **Synchronous 4-Bit Gain Control Output**
- **Internal 1.2-V Level Detector for Receive**
- **TTL-Compatible**
- **Interfaces to Electrostatic or Piezoelectric Transducers**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL851 is an economical digital I^2L ranging control integrated circuit designed for use with the Texas Instruments TL852 Sonar ranging receiver integrated circuit.

The TL851 is designed for distance measurement from six inches to 35 feet. The device has an internal oscillator that uses a low-cost external ceramic resonator. With a simple interface and a 420-kHz ceramic resonator, the device will drive a 50-kHz electrostatic transducer.

The device cycle begins when Initiate (INIT) is taken to the high logic level. There must be at least 5 ms from initial power up (V_{CC}) to the first initiate signal in order for all the device internal latches to reset and for the ceramic-resonator-controlled oscillator to stabilize. The device will transmit a burst of 16 pulses each time INIT is taken high.

The oscillator output (OSC) is enabled by INIT. The oscillator frequency is the ceramic resonator frequency divided by 8.5 for the first 16 cycles (during transmit) and then the oscillator frequency changes to the ceramic resonator frequency divided by 4.5 for the remainder of the device cycle.

When used with an external 420 kilohertz ceramic resonator, the device internal blanking disables the receive input (REC) for 3.8 ms after initiate to exclude false receive inputs that may be caused by transducer ringing. The internal blanking feature also eliminates echos from objects closer than 1.3 feet from the transducer. If it is necessary to detect objects closer than 1.3 feet, then the internal blanking may be shortened by taking the blanking inhibit (BINH) high, enabling the receive input. The blanking input (BLNK) may be used to disable the receive input and reset ECHO to a low logic level at any time during the device cycle for selective echo exclusion or for a multiple-echo mode of operation.

The device provides a synchronous 4-bit gain control output (12 steps) designed to control the gain of the TL852 sonar ranging receiver integrated circuit. The digital gain control waveforms are shown in Figure 2 with the nominal transition times from INIT listed in the Gain Control Output Table.

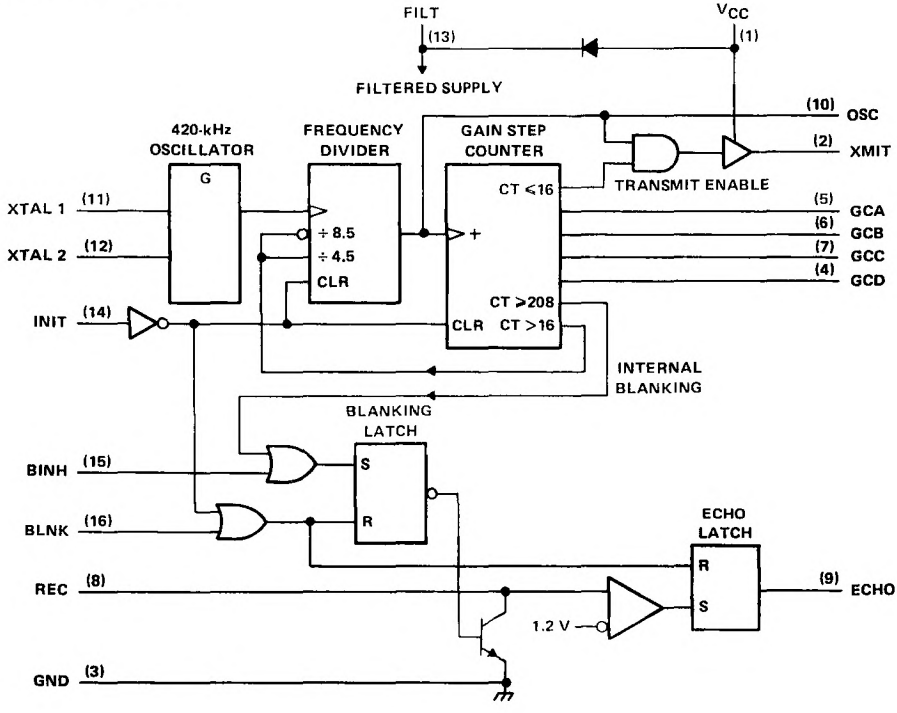
The threshold of the internal receive level detector is 1.2 volts. The TL851 operates over a supply voltage range of 4.5 volts to 6.8 volts and is characterized for operation from 0°C to 40°C.

GAIN CONTROL OUTPUT TABLE

STEP NUMBER	GCD	GCC	GCB	GCA	TIME (ms) FROM INITIATE ††
0	L	L	L	L	2.38 ms
1	L	L	L	H	5.12 ms
2	L	L	L	L	7.87 ms
3	L	L	H	H	10.61 ms
4	L	H	L	L	13.35 ms
5	L	H	L	H	16.09 ms
6	L	H	H	L	18.84 ms
7	L	H	H	H	21.58 ms
8	H	L	L	L	27 07 ms
9	H	L	L	H	32.55 ms
10	H	L	H	L	38.04 ms
11	H	L	H	H	INIT ↓

† This is the time to the end of the indicated step and assumes a nominal 420-kHz ceramic resonator.

functional block diagram



4 Special Functions

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

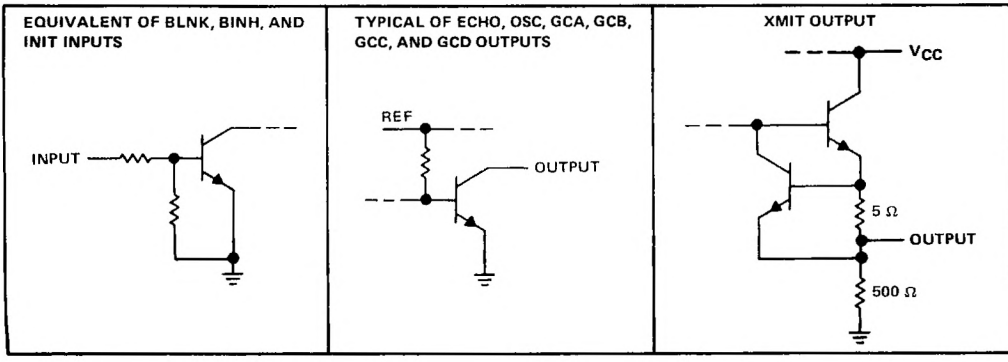
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, [illegible] INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, [illegible] INIT		0.6	V
Delay time, power up to [illegible] high		5		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	ECHO, OSC, GCA, [illegible] GCC, GCD	V_{OH} = 5.5 V			100	μA
Low-level output voltage, V_{OL}	[illegible] OSC, GCA, [illegible] GCC, GCD	I_{OL} = 1.6 mA			0.4	V
On-state output current	[illegible] output	V_O = 1 V		−140		mA
Internal blanking interval	[illegible] input			[illegible]‡		ms
Frequency during 16-pulse transmit period	[illegible] output			[illegible]		kHz
	XMIT output			49.4‡		
Frequency after 16-pulse transmit period	[illegible] output			93.3‡		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				260	mA
	After transmit period				55	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
‡These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



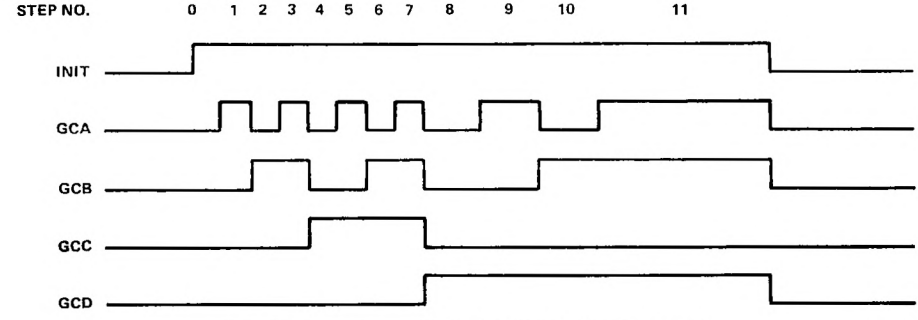


FIGURE 1. DIGITAL GAIN CONTROL WAVEFORMS

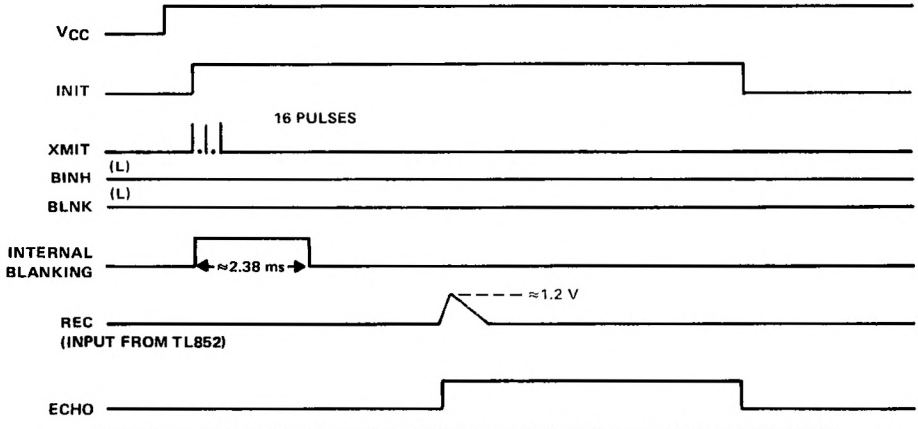


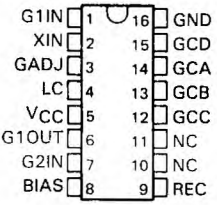
FIGURE 2. EXAMPLE OF SINGLE-ECHO-MODE CYCLE WHEN USED WITH THE TL852 RECEIVER AND 420-kHz CERAMIC RESONATOR

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2779, SEPTEMBER 1983—REVISED MARCH 1988

- **Designed for Use with the TL851 in Sonar Ranging Modules Like the SN28827**
- **Digitally Controlled Variable-Gain Variable-Bandwidth Amplifier**
- **Operational Frequency Range of 20 kHz to 90 kHz**
- TTL-Compatible
- **Operates from Power Sources of 4.5 V to 6.8 V**
- **Interfaces to Electrostatic or Piezoelectric** Transducers
- **Overall Gain Adjustable with One External Resistor**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TL852 is an economical sonar ranging receiver integrated circuit for use with the TL851 control integrated circuit. A minimum of external components is required for operation, and this amplifier easily interfaces to Polaroid's 50-kilohertz electrostatic transducer. An external 68-kilohm ±5% resistor from pin 8 (Bias) to pin 16 (GND) provides the internal biasing reference. Amplifier gain can be set with a resistor from pin 1 (G1IN) to pin 3 (GADJ). Required amplifier gain will vary for different applications. Using the detect-level measurement circuit of Figure 1, a nominal peak-to-peak value of 230 millivolts input during gain step 2 is recommended for most applications. For reliable operation, a level no lower than 50 millivolts should be used. The recommended detect level of 230 millivolts can be obtained for most amplifiers with an R1 value between 5 kilohms and 20 kilohms.

Digital control of amplifier gain is provided with gain control inputs on pins 12 through 15. These inputs must be driven synchronously (all inputs stable within 0.1 microsecond) to avoid false receive output signals due to invalid logic counts. This can be done easily with the TL851 control IC. A plot showing relative gain for the various gain steps versus time can be seen in Figure 2. To dampen ringing of the 50-kilohertz electrostatic transducer, a 5-kilohm resistor from pin 1 (GAIN) to pin 2 (XIN) is recommended.

An external parallel combination of inductance and capacitance between pin 4 (LC) and pin 5 (V_{CC}) provides an amplifier with an externally controlled gain and Q. This not only allows control of gain to compensate for attenuation of signal with distance, but also maximizes noise and sidelobe rejection. Care must be taken to accurately tune the L-C combination at operating frequency or gain and Q will be greatly reduced at higher gain steps.

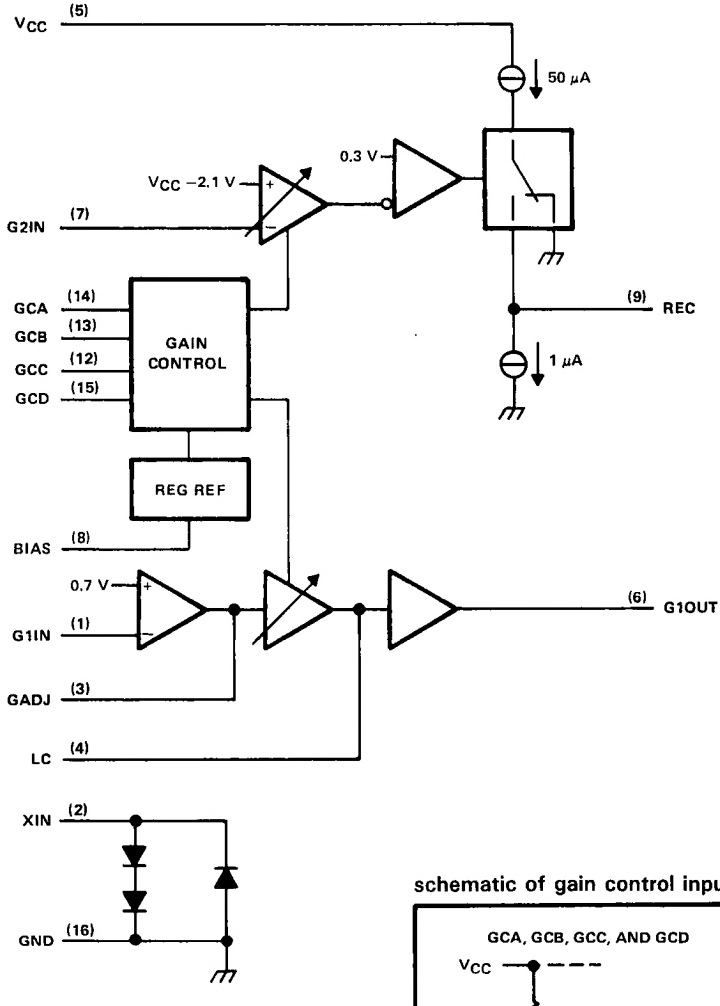
AC coupling between stages of the amplifier is accomplished with a 0.01-microfarad capacitor for proper biasing.

The receive output is normally held at a low level by an internal 1-microampere current source. When an input of sufficient amplitude is received, the output is driven alternately by the 1-microampere discharge current and a 50-microampere charging current. A 1000-picofarad capacitor is required from the receive output (pin 9) to ground (pin 16) to integrate the received signal so that one or two noise pulses will not be recognized.

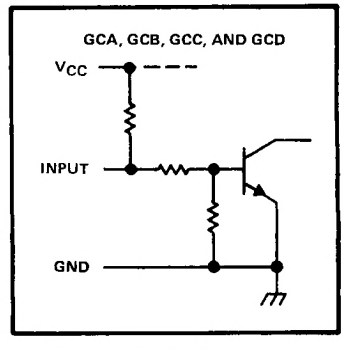
Pin 2 (XIN) provides clamping for the transformer secondary when used for transducer transmit drive as shown in Figure 4 of the SN28827 data sheet.

The TL852 is characterized for operation from 0°C to 40°C

functional block diagram



schematic of gain control inputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
XIN input current (50% duty cycle) . . . . . ±60 mA
Continuous power dissipation at (or below) 25 °C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . −40 °C to 85 °C
Storage temperature range . . . . . −65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260 °C

NOTE 1: For operation above 25 °C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	GCA, GCB, GCC, GCD	2.1		V
Low-level input voltage, V_{IL}			0.6	V
Bias resistor between pins 8 and 16		64	72	kΩ
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

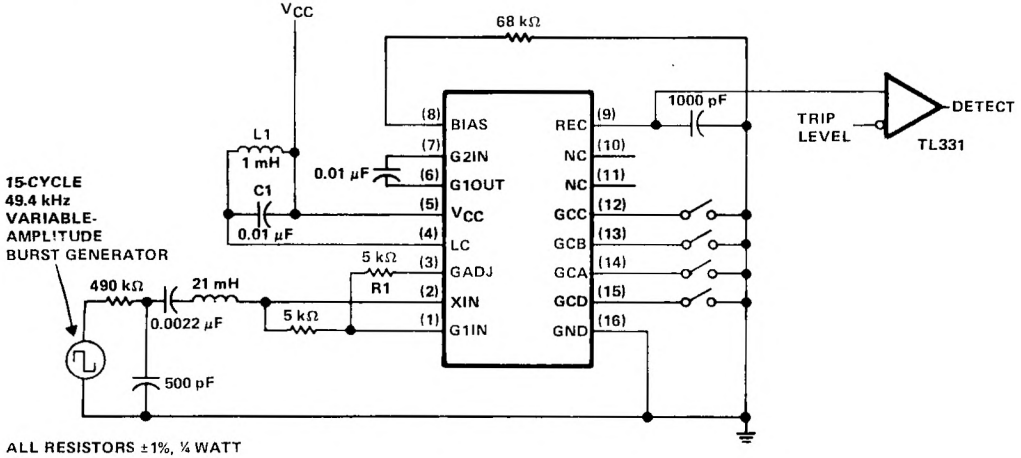
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input clamp voltage at XIN	I_I = 40 mA				2.5	V
	I_I = −40 mA				−1.5	
Open-circuit input voltage at GCA, GCB, GCC, GCD	V_{CC} = 5 V,	I_I = 0		2.5		V
High-level input current, I_{IH}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IH} = 2 V		−0.5		mA
Low-level input current, I_{IL}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IL} = 0			−3	mA
Receive output current	I_{G2IN} = −100 μA,	V_O = 0.3 V		1		μA
	I_{G2IN} = 100 μA,	V_O = 0.1 V		−50		
Supply current, I_{CC}					45	mA

†Typical values are at V_{CC} = 5 V and T_A = 25 °C.

TYPICAL APPLICATION INFORMATION

detect level vs gain step

Detect level is measured by applying a 15-cycle burst of 49.4 kilohertz square wave just after the beginning of the gain step to be tested. The least burst amplitude that makes the REC pin reach the trip level is defined to be the detect level. System gain is then inversely proportional to detect level. See the test circuit in Figure 1.



ALL RESISTORS ±1%, ¼ WATT
ALL CAPACITORS ±1%, FILM
L1 Q > 60 at 50 kHz
C1 Q > 500 at 50 kHz

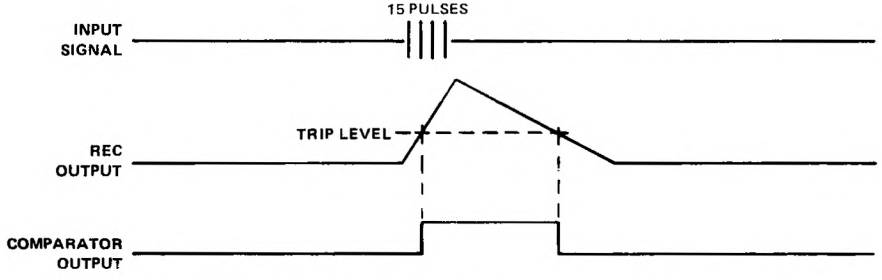


FIGURE 1. DETECT-LEVEL MEASUREMENT CIRCUIT AND WAVEFORMS

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TYPICAL APPLICATION INFORMATION

GAIN STEP TABLE

GCD	GCC	GCB	GCA	STEP NUMBER
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11

RECEIVER GAIN
vs
GAIN STEP NUMBERS

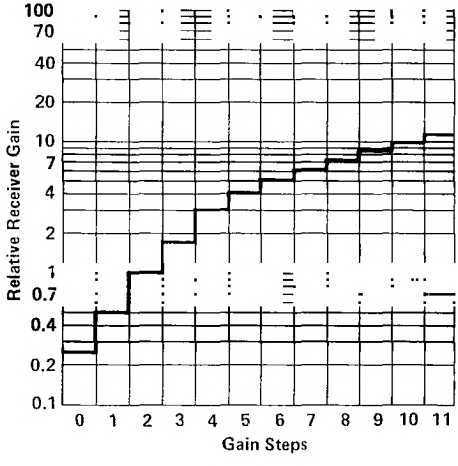
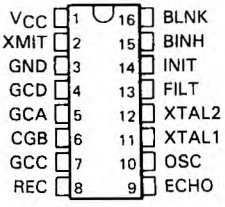


FIGURE 2

D2843, DECEMBER 1984—REVISED MARCH 1988

- **Designed for Use with the TL852 in Sonar Ranging Modules Like the SN28828**
- **Operates with Single Supply**
- **Accurate Clock Output for External Use**
- **Synchronous 4-Bit Gain Control Output**
- **Internal 1.2-V Level Detector for Receive**
- **TTL-Compatible**
- **Interface to 40-kHz Piezoelectric or Electrostatic Transducers**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL853 is an economical digital I^2L ranging control integrated circuit designed for use with the Texas Instruments TL852 Sonar ranging receiver integrated circuit.

The TL853 is designed for distance measurement ranging from six inches to 35 feet. The device has an internal oscillator that uses a low-cost external ceramic resonator. With a simple interface and a 420-kHz ceramic resonator, the device will drive a 40-kHz piezoelectric transducer.

The device cycle begins when Initiate (INIT) is taken to the high logic level. There must be at least 5 ms from initial power up (V_{CC}) to the first initiate signal in order for all the device internal latches to reset and for the ceramic-resonator-controlled oscillator to stabilize. The device will transmit a burst of 16 pulses each time INIT is taken high.

The oscillator output (OSC) is enabled by INIT. The oscillator frequency is the ceramic resonator frequency divided by 10.5 for the first 16 cycles (during transmit) and then the oscillator frequency changes to the ceramic resonator frequency divided by 4.5 for the remainder of the device cycle.

When used with an external 420-kilohertz ceramic resonator, the device internal blanking disables the receive input (REC) for 2.46 ms after initiate to exclude false receive inputs that may be caused by transducer ringing. The internal blanking feature also eliminates echos from objects closer than 1.37 feet from the transducer. If it is necessary to detect objects closer than 1.37 feet, then the internal blanking may be shortened by taking the blanking inhibit (BINH) high, enabling the receive input. The blanking input (BLNK) may be used to disable the receive input and reset ECHO to a low logic level at any time during the device cycle for selective echo exclusion or for a multiple-echo mode of operation.

The device provides a synchronous 4-bit gain control output (12 steps) designed to control the gain of the TL852 sonar ranging receiver integrated circuit. The digital gain control waveforms are shown in Figure 2 with the nominal transition times from INIT listed in the Gain Control Output Table.

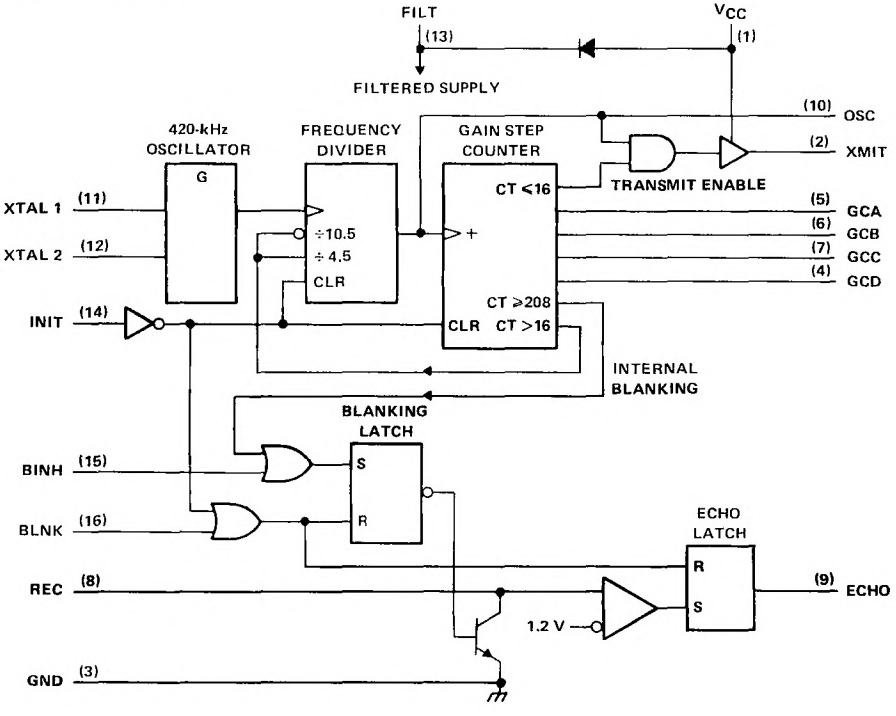
The threshold of the internal receive level detector is 1.2 volts. The TL853 operates over a supply voltage range of 4.5 volts to 6.8 volts and is characterized for operation from 0°C to 40°C.

GAIN CONTROL OUTPUT TABLE

STEP NUMBER	CGD	GCC	GCB	GCA	TIME (ms) FROM INITIATE††
0	L	L	L	L	2.46 ms
1	L	L	L	H	5.2 ms
2	L	L	H	L	7.94 ms
3	L	L	H	H	10.69 ms
4	L	H	L	L	13.43 ms
5	L	H	L	H	16.17 ms
6	L	H	H	L	18.91 ms
7	L	H	H	H	21.66 ms
8	H	L	L	L	27.14 ms
9	H	L	L	H	32.63 ms
10	H	L	H	L	38.11 ms
11	H	L	H	H	INIT ↓

†This is the time to the end of the indicated step and assumes a nominal 420-kHz ceramic resonator.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
Continuous power dissipation at (or below) 25 °C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

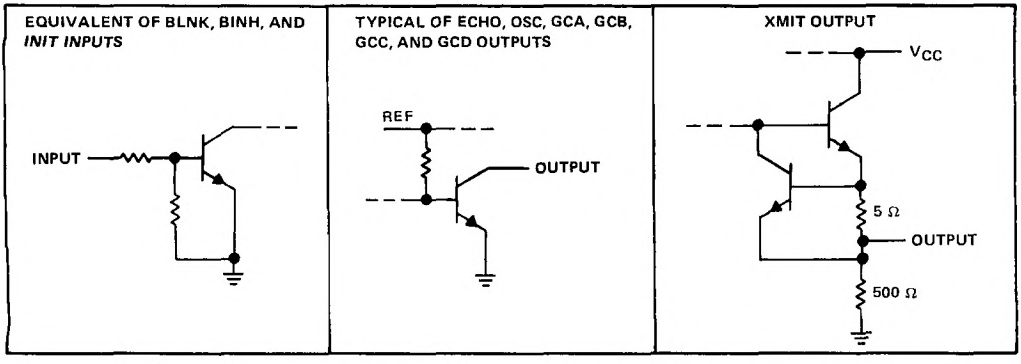
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
Delay time, power up to [illegible] high		5		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current		[illegible] INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}		[illegible] GCA, GCB, [illegible] GCD	V_{OH} = 5.5 mA			100	μA
Low-level output voltage, V_{OL}		ECHO, [illegible] GCA, [illegible] GCC, GCD	I_{OL} = 1.6 mA			0.4	V
On-state output current		[illegible] output	V_O = 1 V		−140		mA
Internal blanking interval		F[illegible] input			2.46‡		ms
Frequency during 16-pulse transmit period		[illegible] output			40‡		kHz
		[illegible] output			40‡		
Frequency after 16-pulse transmit period		OSC output			93.3‡		kHz
		XMIT output			0		
Supply current, I_{CC}	During transmit period					260	mA
	After transmit period					55	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
‡These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



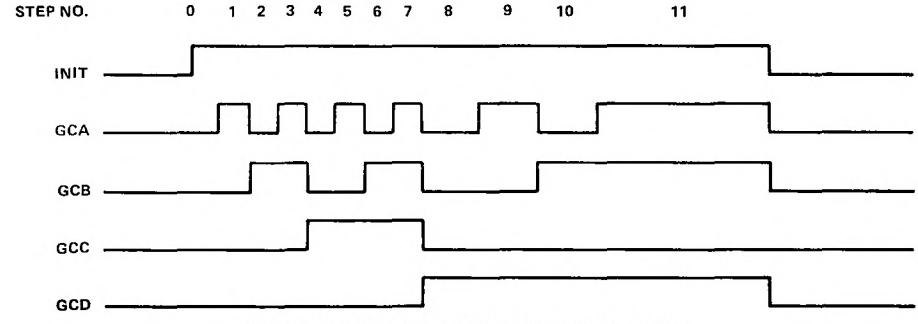


FIGURE 1. DIGITAL GAIN CONTROL WAVEFORMS

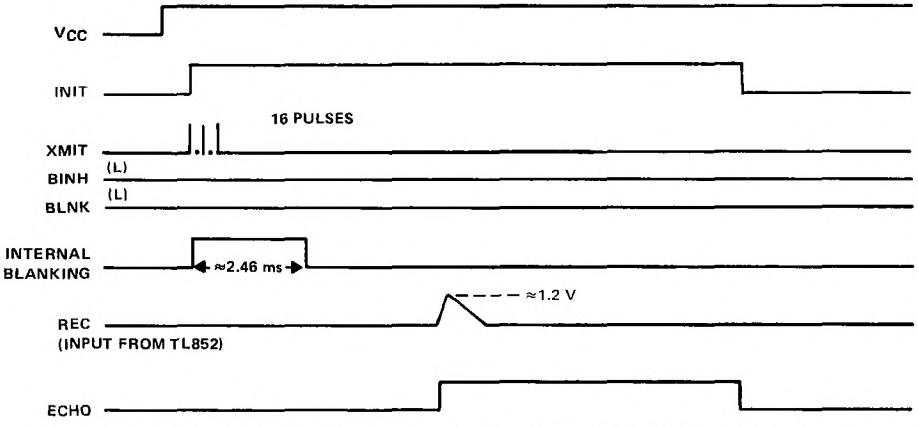


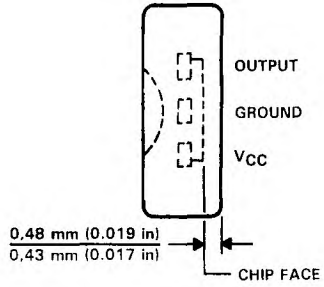
FIGURE 2. EXAMPLE OF SINGLE-ECHO-MODE CYCLE WHEN USED WITH THE TL852 RECEIVER AND 420-kHz CERAMIC RESONATOR

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2903, SEPTEMBER 1985—REVISED APRIL 1988

- **Magnetic-Field Sensing Hall-Effect Input**
- **On-Off Hysteresis**
- **Small Size**
- **Standard Bipolar Technology Minimizes ESD Susceptibility**
- **I_{OL} . . . 20 mA Min at V_{OL} = 0.4 V**
- **I_{OH} . . . 1 μA Max at V_{OH} = 24 V**
- **Buried Hall-Effect Cell Reduces Threshold Drift Caused by Temperature Variation and Aging**
- **Direct Replacement for the Sprague UGN3013**

LU PACKAGE
(TOP VIEW)



description

The TL3013C is a low-cost magnetically operated electronic switch that utilizes the Hall effect to sense magnetic fields. Each circuit consists of a Hall-effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

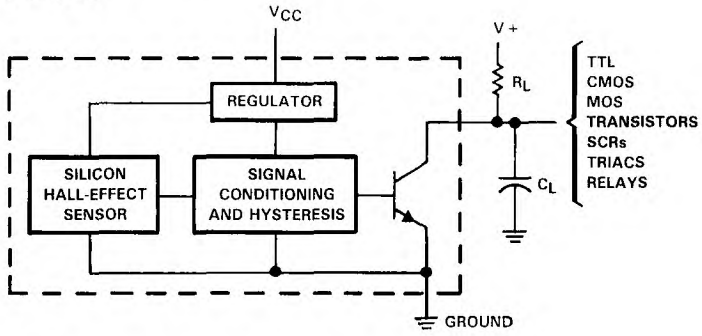
The TL3013C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE (0°C ≤ T_A ≤ 70°C)

FLUX DENSITY	OUTPUT
B ≤ 2.5 mT (25 G)	Off
2.5 mT (25 G) < B < 45 mT (450 G)	Undefined
B ≥ 45 mT (450 G)	On

The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in millitesla may be converted to gauss (G) by multiplying by ten.

functional block diagram



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Output voltage . . . . . 40 V
Output current . . . . . 30 mA
Magnetic flux density . . . . . unlimited
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1. Voltage values are with respect to the network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{OP}	Operate-point magnetic flux density (see Figure 2)			30	45	mT†
B_{RP}	Release-point magnetic flux density (see Figure 2)		2.5	22.5		mT†
B_{hys}	Hysteresis ($B_{OP} - B_{RP}$)		3	7.5		mT†
α_B	Temperature coefficient of B_{OP} and B_{RP}			±0.25		%/°C
V_{OL}	Low-level output voltage	I_{OL} = 20 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 24 V			1	μA
I_{CC}	Supply current			3	7	mA

†The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

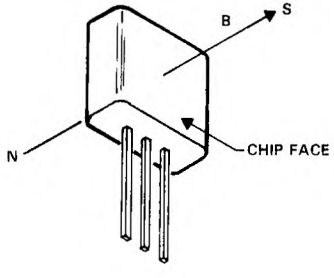


FIGURE 1. DEVICE ORIENTATION IN A MAGNETIC FIELD

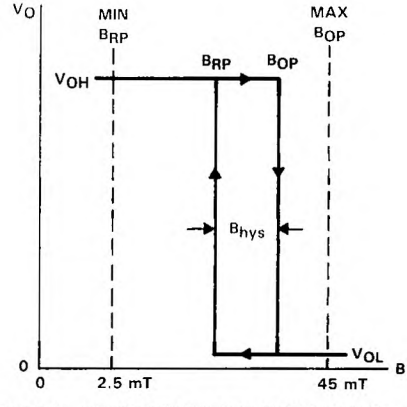


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

switching characteristics at V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	R_L = 820 Ω, C_L = 20 pF		350		ns
t_f	Output fall time			85		

TEXAS INSTRUMENTS
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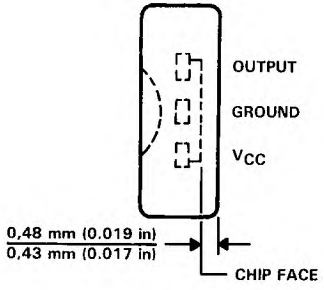
D2903, JULY 1985—REVISED

- **Magnetic-*Field* Sensing Hall-Effect Input**
- **On-Off Hysteresis**
- Small Size
- **Standard Bipolar Technology Minimizes ESD Susceptibility**
- **I_{OL} . . . 20 mA Min at V_{OL} = 0.4 V**
- **I_{OH} . . . 1 μA Max at V_{OH} = 24 V**
- **Buried Hall-Effect Cell Reduces Threshold Drift Caused by Temperature Variation and Aging**
- **Direct Replacement for the Sprague UGN3019**

LU PACKAGE
(TOP VIEW)



description

The TL3019C is a low-cost magnetically operated electronic switch that utilizes the Hall Effect to sense magnetic fields. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

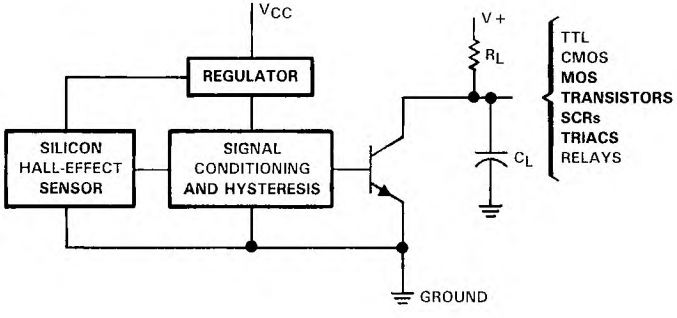
The TL3019C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE (0°C ≤ T_A ≤ 70°C)

FLUX DENSITY	OUTPUT
B ≤ 12.5 mT (125 G)	Off
12.5 mT (125 G) < B < 50 mT (500 G)	Undefined
B ≥ 50 mT (500 G)	On

The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Output voltage . . . . . 40 V
Output current . . . . . 30 mA
Magnetic flux density . . . . . unlimited
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1. Voltage values are with respect to the network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{OP}	Operate-point magnetic flux density (see Figure 2)			42	50	mT†
B_{RP}	Release-point magnetic flux density (see Figure 2)		12.5	30		mT†
B_{hys}	Hysteresis ($B_{OP}-B_{RP}$)		5	12		mT†
α_B	Temperature coefficient of B_{OP} and B_{RP}			±0.25		%/°C
V_{OL}	Low-level output voltage	I_{OL} = 20 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 24 V			1	μA
I_{CC}	Supply current			3	7	mA

†The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

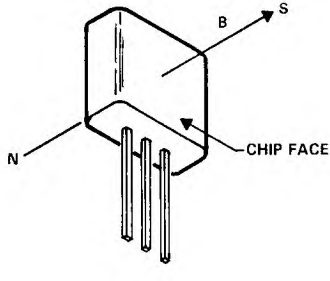


FIGURE 1. DEVICE ORIENTATION IN A MAGNETIC FIELD

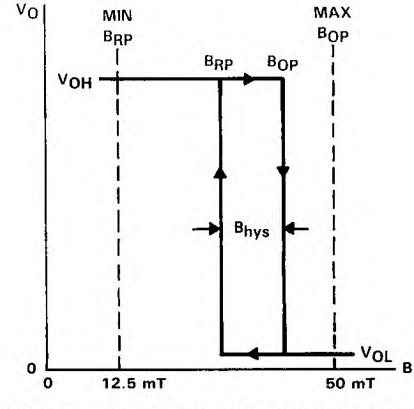


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

switching characteristics at V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	R_L = 820 Ω, C_L = 20 pF		350		ns
t_f	Output fall time			85		

TEXAS INSTRUMENTS
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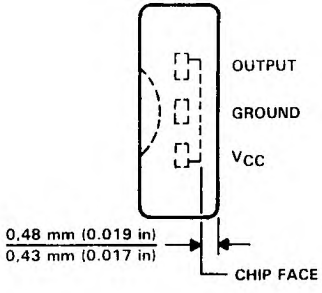
D2903, OCTOBER 1985—REVISED APRIL 1988

- **Magnetic-Field Sensing Hall-Effect Input**
- On-Off Hysteresis
- Small Size
- **Standard Bipolar Technology Minimizes ESD Susceptibility**
- **I_{OL} . . . 20 mA Min at V_{OL} = 0.4 V**
- **I_{OH} . . . 1 μA Max at V_{OH} = 24 V**
- **Buried Hall-Effect Cell Reduces Threshold Drift Caused by Temperature Variation and Aging**
- **Direct Replacement for the Sprague UGN3020**

LU PACKAGE
(TOP VIEW)



description

The TL3020C is a low-cost magnetically operated electronic switch that utilizes the Hall effect to sense magnetic fields. Each circuit consists of a Hall-effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

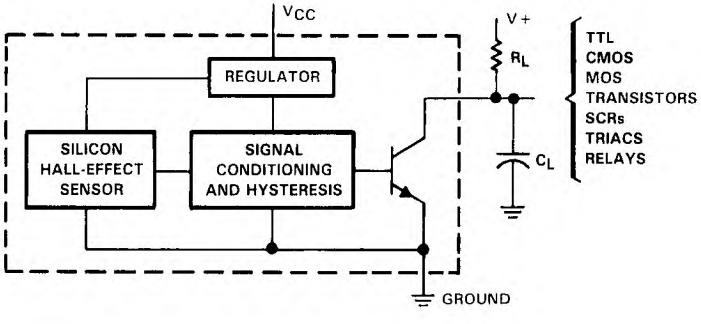
The TL3020C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE (0°C ≤ T_A ≤ 70°C)

FLUX DENSITY	OUTPUT
B ≤ 5 mT (50 G)	Off
5 mT (50 G) < B < 35 mT (350 G)	Undefined
B ≥ 35 mT (350 G)	On

The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Output voltage . . . . . 40 V
Output current . . . . . 30 mA
Magnetic flux density . . . . . unlimited
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1. Voltage values are with respect to the network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{OP}	Operate-point magnetic flux density (see Figure 2)			22	35	mT†
B_{RP}	Release-point magnetic flux density (see Figure 2)		5	16.5		mT†
B_{hys}	Hysteresis ($B_{OP} - B_{RP}$)		2	5.5		mT†
α_B	Temperature coefficient of B_{OP} and B_{RP}			±0.25		%/°C
V_{OL}	Low-level output voltage	I_{OL} = 20 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 24 V			1	μA
I_{CC}	Supply current			3	7	mA

†The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

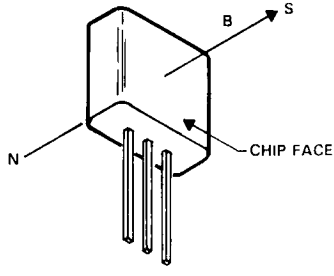


FIGURE 1. DEVICE ORIENTATION IN A MAGNETIC FIELD

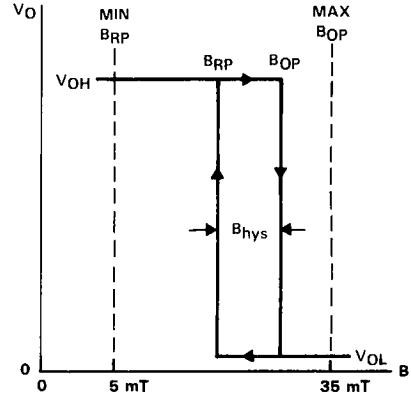


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

switching characteristics at V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

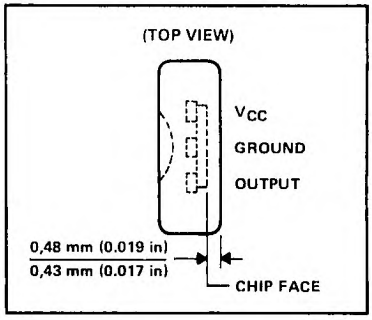
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	R_L = 820 Ω, C_L = 20 pF				ns
t_f	Output fall time					

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

APRIL 1985—REVISED APRIL 1988

- Magnetic-Field Sensing Hall-Effect Input
- On-Off Hysteresis
- Small Size
- Solid-State Technology
- Open-Collector Output
- Buried Hall-Effect Cell Reduces Threshold Drift Caused By Temperature Variation and Aging

LU PACKAGE



description

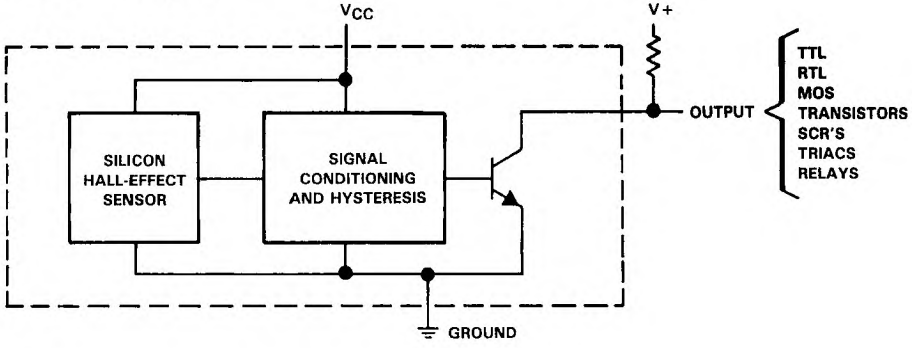
The TL3101I and TL3101C are low-cost magnetically operated electronic switches that utilize the Hall Effect to sense steady-state magnetic fields. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

The TL3101C is characterized for operation over the temperature range of 0°C to 70°C. The TL3101I is characterized for operation over the range of −20°C to 85°C.

FUNCTION TABLE $0°C \geq T_A \leq 70°C$

FLUX DENSITY	OUTPUT
≤ −25 mT	Off
−25 mT < B < 25 mT	Undefined
≥ 25 mT	On

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

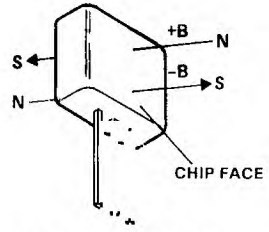
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Output voltage . . . . . 30 V
Output current . . . . . 20 mA
Operating free-air temperature range: TL3101C . . . . . 0°C to 70°C
TL3101I . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Magnetic flux density . . . . . unlimited

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V ± 5% (unless otherwise noted)

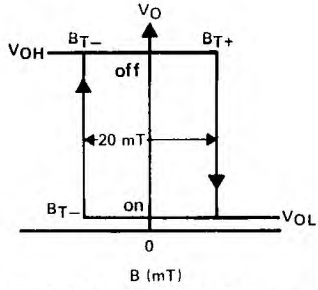
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
B_{T+}	Threshold of positive going magnetic flux density†			0°C to 70°C	0		25	mT§
				−20°C to 85°C	0		35	
B_{T-}	Threshold of negative going magnetic flux density†			0°C to 70°C	−25‡		0	mT§
				−20°C to 85°C	−35‡		0	
$B_{T+} - B_{T-}$	Hysteresis			0°C to 70°C	5	20		mT‡
I_{OH}	High-level output current	V_{OH} = 20 V		0°C to 70°C			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75, I_{OL} = 16 mA		0°C to 70°C			0.4	V
I_{CC}	Supply current	V_{CC} = 5.25 V	Output low	0°C to 70°C			6	mA
			Output high				4	

†Threshold values are those levels of magnetic flux density at which the output changes state. For the TL3101, a level more positive than B_{T+} causes the output to a low level and a level more negative than B_{T-} causes the output to go to a high level. See Figures 1 and 2.
‡The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for flux density threshold levels only.
§The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY



The positive-going threshold (B_{T+}) is a positive B level at which a positive-going flux density results in the TL3101 output turning on. The negative-going threshold is negative B level at which a negative-going flux density results in the TL3101 turning off.

FIGURE 2. REPRESENTATIVE CURVES OF V_O vs B

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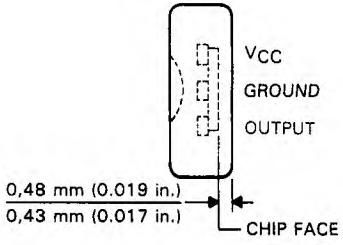
D3184, MAY 1985—REVISED FEBRUARY 1989

- **Output Voltage Linear with Applied Magnetic Field**
- **Sensitivity Stable Over Wide Operating Temperature Range**
- **Buried Hall Cell Reduces Changes Due to Temperature Variation and Aging**
- **Solid-State Technology**
- **Three-Terminal Device**
- **Senses Static or Dynamic Magnetic Fields**

LU PACKAGE
(TOP VIEW)

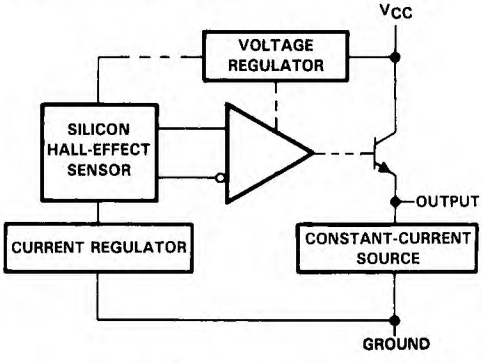


description

The TL3103I and TL3103C are low-cost magnetic-field sensors designed to provide a linear output voltage proportional to the magnetic field they sense. These monolithic circuits incorporate a Hall element as the primary sensor along with a voltage reference and a precision amplifier. Temperature stabilization and internal trimming circuitry yield a device that features high overall sensitivity accuracy with less then 5% error over its operating temperature range.

The TL3103I is characterized for operation from −20°C to 85°C. The TL3103C is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	775 mW
Operating free-air temperature range: TL3103I	−20°C to 85°C
TL3103C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Magnetic flux density	unlimited

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C.

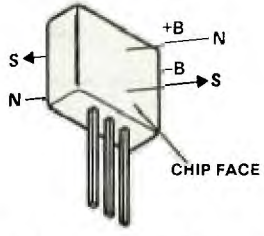
recommended operating conditions

		TL3103I			TL3103C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		9	12	15	9	12	15	V
Magnetic flux density, B				±50			±50	mT
Output current, I_O	Sink			0.5			0.5	mA
	Source			−2			−2	
Operating free-air temperature, T_A		−20		85	0		70	°C

electrical characteristics over recommended ranges of supply voltage and magnetic flux density, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_O	Output voltage	I_O = −2 mA to 0.5 mA, B = 0 mT§	5.8	6	6.2	V
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)			18		mV/V
S	Magnetic sensitivity ($\Delta V_O/\Delta B$)	B = −50 to 50 mT§	14	16	18	V/T§
ΔS	Magnetic sensitivity change with temperature	ΔT_A = 25°C to MIN or MAX			±5	%
I_{CC}	Supply current	B = 0 mT§, I_O = 0		8	12	mA
f_{max}	Maximum operating frequency			100		kHz

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Typical values are at V_{CC} = 12 V at T_A = 25°C.
§The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in millitesias may be converted to gauss by multiplying by ten, e.g., 50 millitesla = 500 gauss.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY

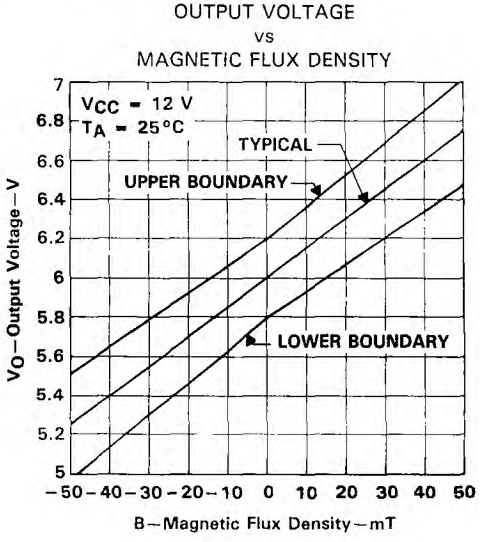


FIGURE 2

4 Special Functions

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TYPICAL APPLICATION DATA

The circuit in Figure 3 may be used to set the output voltage at zero field strength to exactly 6 V (using R1) and to set the sensitivity to exactly −15 V/T (using R2) as depicted in Figure 4.

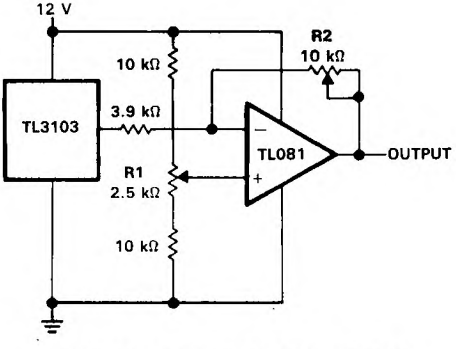

FIGURE 3. COMPENSATION CIRCUIT

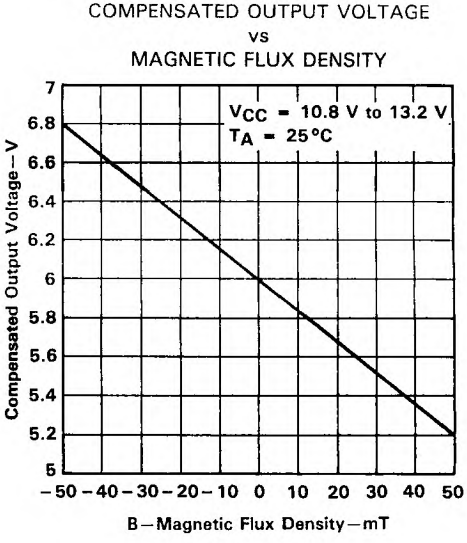

FIGURE 4

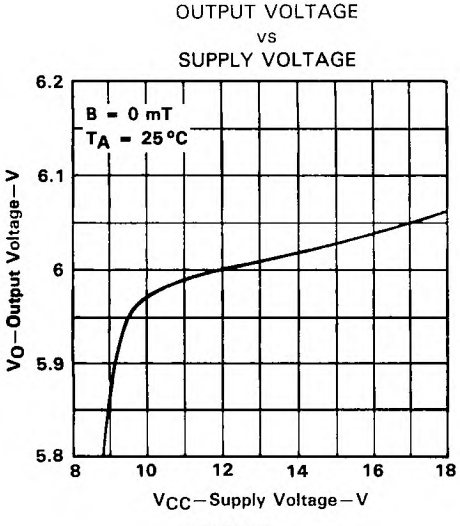

FIGURE 5

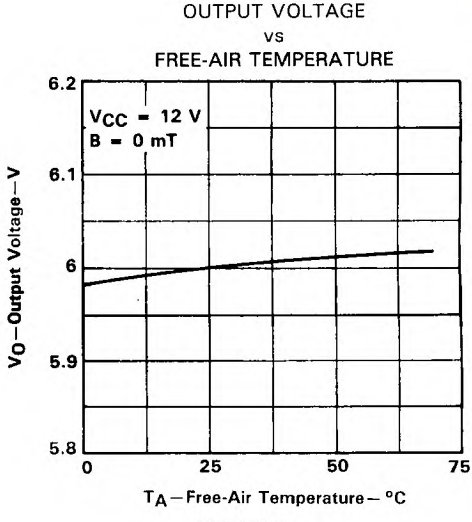

FIGURE 6

TYPICAL APPLICATION DATA

MAGNETIC SENSITIVITY
vs
SUPPLY VOLTAGE

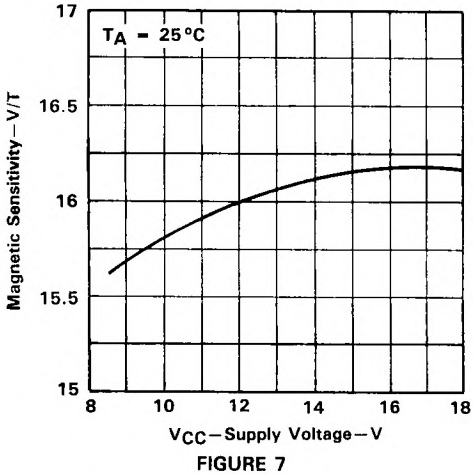

FIGURE 7

MAGNETIC SENSITIVITY
vs
FREE-AIR TEMPERATURE

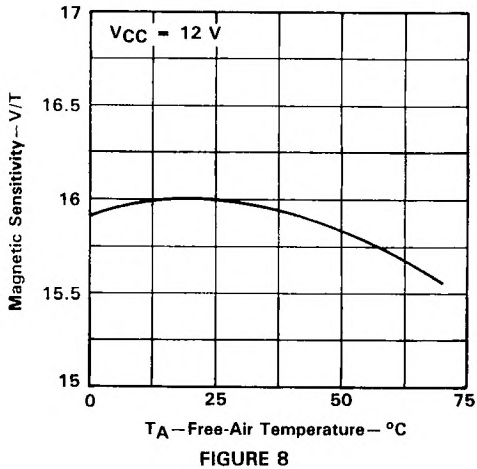

FIGURE 8

linear hall-effect sensor in isolated feedback applications

purpose

The purpose of the circuit in Figure 9 is to demonstrate the capability of the linear hall-effect sensor to provide isolated sensing.

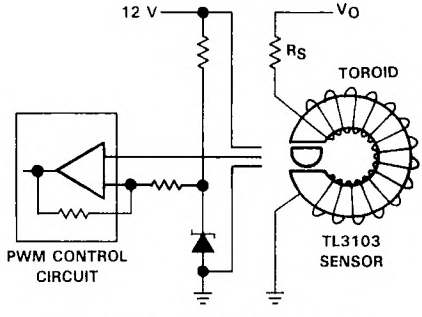

FIGURE 9. ISOLATE FEEDBACK

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linear sensor

The TL3103 senses the presence of a magnetic field. In the absence of a magnetic field, the TL3103 output voltage is 6 V. As the sensor senses the presence of a magnetic field, its output varies proportionally at 16 V/T.

toroid

The permeability (μ) of any given material is the relationship of the magnetic flux density (B) to the magnetic field intensity (H). The magnetic field intensity of a toroid is given by the expression:

$$H = \frac{NI}{L} \tag{1}$$

Where: NI is number of turns times the current.
L is mean length of the toroid.

The expression for the magnetic flux density then becomes:

$$B = \mu \frac{NI}{L} \tag{2}$$

With an air gap, the basic expression is altered to the following:

$$B_{gap} = \mu_o \frac{NI}{L + Kg} K \tag{3}$$

Where: μ_o is the permeability of air = 12.57×10^{-7}.
K is the relative permeability of the toroid (μ/μ_o).
g is the length of the air gap in mils.

If the relative permeability of the toroid is large (Kg > K), the mean length of the toroid becomes insignificant and the expression for flux density reduces to:

$$B_{gap} = \frac{NI}{g} \tag{4}$$

circuit

As previously discussed, the output of the TL3103 is:

$$V_{sense} = 6\ V + (16\ V/T)\ (\mu_o \frac{NI}{g}) \tag{5}$$

This shows how the output of the TL3103 varies with the ampere turns of the toroid. For some relative numbers, Figure 9 uses an Arnold toroid #A393163-2 with a 156-mil air gap. The magnetic field created in the air gap is:

$$B\ (gauss) = 1.92\ NI\ (ampere\ turns) \tag{6}$$

Therefore, the variation in the output of the TL3103 is:

$$\Delta V_{sense}\ (mV) = (1.6)\ (1.92NI) \tag{7}$$

The sensitivity of the TL3103 to the current in the windings can therefore be altered by the number of turns composing the windings.

ΔV_{sense}	N	ΔI
614 mV	20	10 mA
614 mV	200	1 mA
614 mV	2000	100 μA

power supply application

Since the output of the TL3103 varies proportionally to the current flow in the toroid, this leads to the obvious application of current sensing. The features presented by this approach are as follows:

1. Minimum power loss in the sensing element:

$$P_{loss} = I_2R_{toroid} \quad (R < 0.01\ \Omega \text{ for 20 turns}) \tag{8}$$

2. Isolated feedback, no passive connection required.

Another application of this concept provides a linear isolated feedback of the output voltage. This is accomplished by connecting a resistor in series with the toroid terminated to ground. In this configuration, the current in the toroid is determined by the output voltage ($I_S = V_O/R_S$), therefore, the output variation of the TL3103 is proportional to the output voltage.

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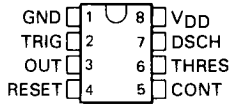
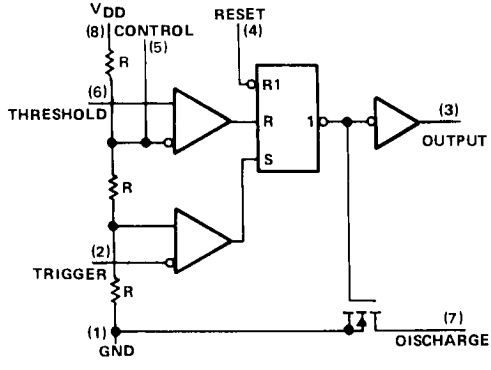
D2791, FEBRUARY 1984—REVISED MAY 1988

- Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V
- Capable of Operation in Astable Mode
- CMOS Output Capable of Swinging Rail to Rail
- High Output-Current Capability
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- Output Fully Compatible with CMOS, TTL, and MOS
- Low Supply Current Reduces Spikes During Output Transitions
- High-Impedance Inputs . . . 10^{12} Ω Typ
- Single-Supply Operation from 1 V to 18 V
- Functionally Interchangeable with the NE555; Has Same Pinout

D OR P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC551 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE555, the TLC551 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC551C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	V_T MAX AT 25°C	PACKAGE	
		SMALL-OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	3.8 V	TLC551CD	TLC551CP

D package is available taped-and-reeled. Add "R" suffix to device type when ordering (i.e. TLC551CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 460 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

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electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		0.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full [illegible]	0.3		1	
Reset current		2[illegible]		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full [illegible]			0.2	
Discharge switch off-state current		2		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		15	100	μA
		Full range			150	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full [illegible]	0.3		1.8	
Reset current		2		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full [illegible]			0.25	
Discharge switch off-state current		2		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		65	[illegible]	μA
		Full range			[illegible]	

†Full range (MIN to MAX) is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		[illegible]		75		
Trigger voltage level		[illegible]	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		170	350	μA
		Full range			500	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		[illegible]		75		
Reset voltage level		[illegible]	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full [illegible]			3.6	
	I_{OL} = 50 mA	2[illegible]		0.63	1	
		Full [illegible]			1.3	
	I_{OL} = 10 mA	2[illegible]		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full [illegible]	13.5			
	I_{OH} = −1 mA	2[illegible]	14.2	14.9		
		Full range	14.2			
Supply current		25°C		[illegible]	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full [illegible]			0.35	
High-level output voltage	I_{OH} = −1 mA	2 [illegible]	17.3	17.9		V
		Full [illegible]	17.3			
Supply current		2 [illegible]		420	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval‡	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 2		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 2	1.2	1.8		MHz

‡Timing interval error is defined as the difference between the measured value and the nominal value of a random sample.
NOTE 2: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

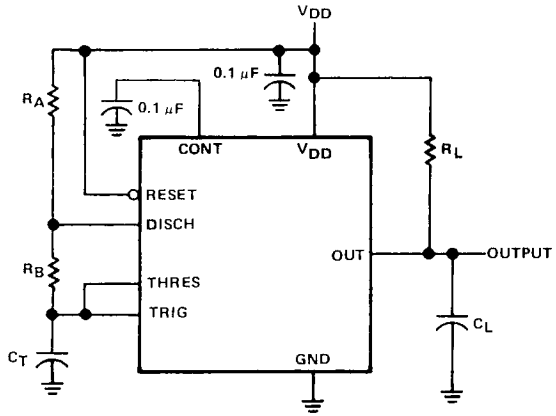


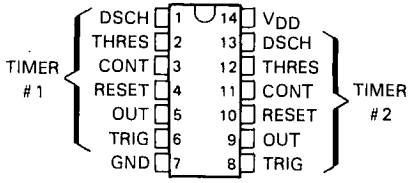
FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

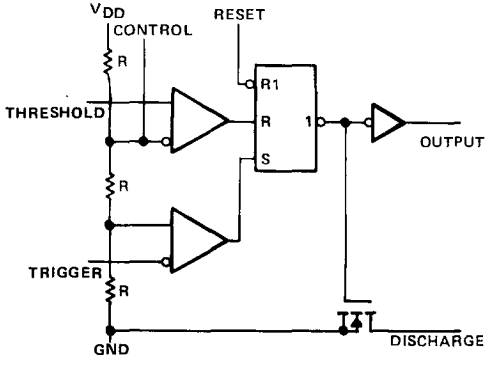
D2796, FEBRUARY 1984—REVISED MAY 1988

- Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V
- Capable of Operation in Astable Mode
- CMOS Output Capable of Swinging Rail to Rail
- High Output-Current Capability
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- Output Fully Compatible with CMOS, TTL, and MOS
- Low Supply Current Reduces Spikes During Output Transitions
- High-Impedance Inputs . . . 10^{12} Ω Typ
- Single-Supply Operation from 1 V to 18 V
- Functionally Interchangeable with the NE556; Has Same Pinout

D OR N PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

description

The TLC552 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC552 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC552 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_T MAX at 25°C
DEVICE	PACKAGE SUFFIX		
TLC552C	D,N	0°C to 70°C	3.8 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e. TLC552CDR)

4 Special Functions

LinCMOS is a trademark of Texas Instruments

description (continued)

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC552C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
N	1150 mW	9.2 mW/°C	25°C

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}		18	V
Operating free-air temperature, T_A	0	70	°C

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electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		1.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		30	200	μA
		Full range			300	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03		V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		130	500	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		340	700	
		Full range			1000	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		0.72	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		0.84	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Initial error of timing interval‡	V_{DD} = 5 V to 15 V,			1%	3%	
Supply voltage sensitivity of timing interval	R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 2			0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF			20	75	ns
Output pulse fall time				15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 2		1.2	2.8		MHz

NOTE 2: R_A, R_B, and C_T are as defined in Figure 1.

‡ Timing interval error is defined as the difference between the measured value and the nominal value of a random sample.

TYPICAL APPLICATION DATA

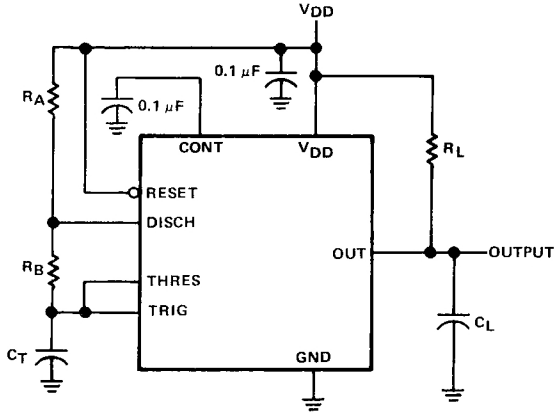


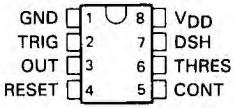
FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

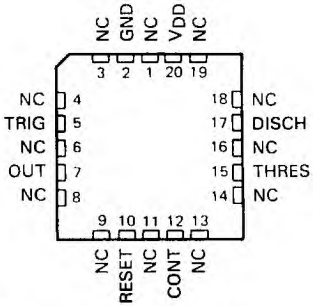
D2784, SEPTEMBER 1983—REVISED OCTOBER 1988

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V**
- **Functionally Interchangeable with the NE555; Has Same Pinout**

TLC555M . . . JG PACKAGE
TLC555I, TLC555C . . . D OR P PACKAGE
(TOP VIEW)



TLC555M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC555 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC555M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC555I is characterized for operation from −40°C to 85°C. The TLC555C is characterized for operation from 0°C to 70°C.

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AVAILABLE OPTIONS

T_A RANGE	V_{CC} RANGE	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 V to 18 V	TLC555CD			TLC555CP
−40°C to 85°C	3 V to 18 V	TLC555ID			TLC555IP
−55°C to 125°C	5 V to 18 V		TLC555MFK	TLC555MJG	

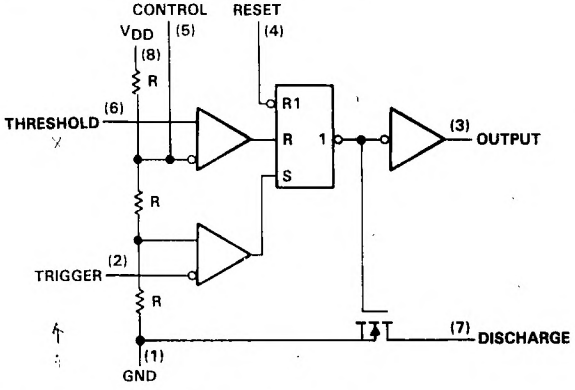
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC555CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irr[illegible]	Irrelevant	Low	On
>MAX	[illegible]	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

functional block diagram



Pin numbers are for all packages except FK.
Reset can override Trigger, which can override Threshold.

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absolute *maximum* ratings over operating free-air temperature range (unless otherwise noted)

		TLC555M	TLC555I	TLC555C	UNIT
Supply voltage (see Note 1)		18	18	18	V
Input voltage		−0.3 to V_{DD}	−0.3 to V_{DD}	−0.3 to V_{DD}	V
Sink current, discherge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation		See Dissipation Rating Table			
Opereting free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package				°C
Leed temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300			
Lead temperature 1,6 mm (1/16 inch) from csse for 10 seconds	D or P package		260	260	

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

electrical characteristics at specified free-air temperature, V_{DD} = 3 V for TLC555I, V_{DD} = 2 V for TLC555C

PARAMETER	TEST CONDITIONS†		TLC555I			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	1.6		2.4	0.95	1.33	1.65	V
		Full range	1.5		2.5	0.85		1.75	
Threshold current		25°C		10			10		pA
		MAX					75		
Trigger voltage level		25°C	0.71		1.29	0.4	0.67	0.95	V
		Full range	0.61		1.39	0.3		1.05	
Trigger current		25°C		10			10		pA
		MAX		150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		2	
Reset current		25°C		10			10		pA
		MAX		150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2		0.03	0.2	V
		Full range			0.375			0.25	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3		0.07	0.3	V
		Full range			0.4			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		1.5	1.9		V
		Full range	2.5			1.5			
Supply current		25°C			250			250	μA
		Full range						400	

†Full range (MIN to MAX) is −40°C to 85°C for TLC555I and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5		0.14	0.5		0.14	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			120			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply current	See Note 2	25°C		170	350		170	350		170	350	μA
		Full range			700			600			500	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I, and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC555M			TLC555I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX					150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7		0.77	1.7		0.77	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			120			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			14.2			
Supply current	See Note 2	25°C		360	600		360	600		360	600	μA
		Full range			1000			900			800	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I, and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5		0.72	1.5		0.72	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
				120			120			0.5		
Low-level output voltage	I_{OL} = 3.2 mA			0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current	See Note 2	25°C			600			600			600	μA
		Full range						900			800	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I, and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configuration in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

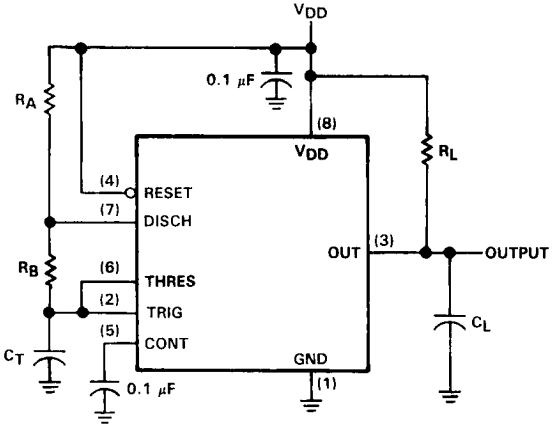
operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval‡	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA



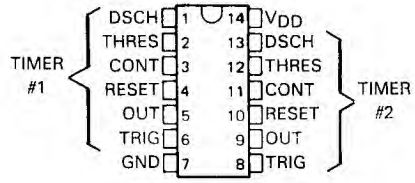
Pin numbers are for all packages except FK.

FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

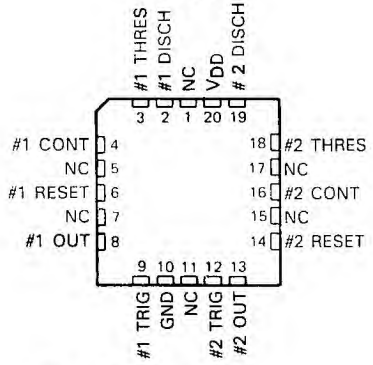
D2796, FEBRUARY 1984—REVISED OCTOBER 1988

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- High-Impedance Inputs . . . 10^{12} Ω Typ
- **Single-Supply Operation from 2 V to 18 V**
- **Functionally Interchangeable with the NE556; Has Same Pinout**

TLC556M . . . J PACKAGE
TLC556I, TLC556C . . . D OR N PACKAGE
(TOP VIEW)



TLC0556M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC556 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC556I is characterized for operation from −40°C to 85°C. The TLC556C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A RANGE	V_{CC} RANGE	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	2 V to 18 V	TLC556CD			TLC556CN
−40°C to 85°C	3 V to 18 V	TLC556ID			TLC556IN
−55°C to 125°C	5 V to 18 V		TLC556MFK	TLC556MJ	

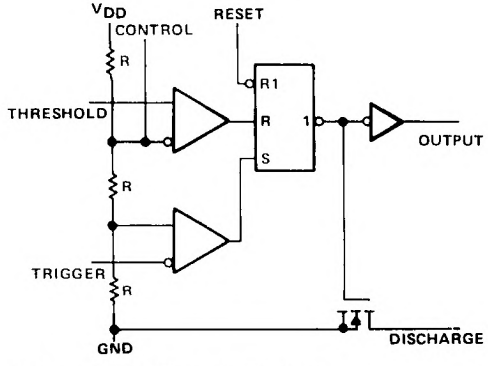
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC556CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC556M	TLC556I	TLC556C	UNIT
Supply voltage (see Note 1)		18	18	18	V
Input voltage		−0.3 to V_{DD}	−0.3 to V_{DD}	−0.3 to V_{DD}	V
Sink current, discharge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300			
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	[illegible] mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	N/A

electrical characteristics at specified free-air temperature, V_{DD} = 3 V for TLC556I, V_{DD} = 2 V for TLC556C

PARAMETER	TEST CONDITIONS†		TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	1.6	2.0	2.4	0.95	1.33	1.65	V
		Full range	1.5		2.5	0.85		1.75	
Threshold current		25°C		10			10		pA
		MAX		150			75		
Trigger voltage level		25°C	0.71	1.0	1.29	0.4	0.67	0.95	V
		Full range	0.61		1.39	0.3		1.05	
Trigger current		25°		10			10		pA
		MAX		[illegible]			75		
Reset voltage level		25°C	0.4	[illegible]	1.5	0.4	1.1	1.5	V
		Full [illegible]	0.3		1.8	0.3		1.8	
Reset current		25		10			10		pA
		MAX		150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2		0.04	[illegible]	V
		Full range			0.375			0.[illegible]	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		[illegible]			0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.0[illegible]	0.3		0.07	0.3	V
		Full [illegible]			0.4			0.35	
High-level output voltage	I_{OH} = −300 μA	2	1.5	1.9		1.5	1.9		V
		Full [illegible]	2.5			1.5			
Supply current		2		130	500		130	500	μA
		Full range			1000			[illegible]	

†Full range (MIN to MAX) is −40°C to 85°C for TLC556I and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX					150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.15	0.5		0.15	0.5		0.15	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply current	See Note 2	25°C		340	700		340	700		340	700	μA
		Full range			1400			1000			1000	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.8	1.7		0.8	1.7		0.8	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			14.2			
Supply current	See Note 2	25°C		0.72	1.2		0.72	1.2		0.72	1.2	mA
		Full range			2			1.8			1.6	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

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electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.73	1.5		0.73	1.5		0.73	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current	See Note 2	25°C			1.2			1.2			1.2	mA
		Full range			2			1.8			1.6	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configuration in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval†	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		1%	3%	
Supply voltage sensitivity of timing interval			0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

†Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A, R_B, and C_T are as defined in Figure 3.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

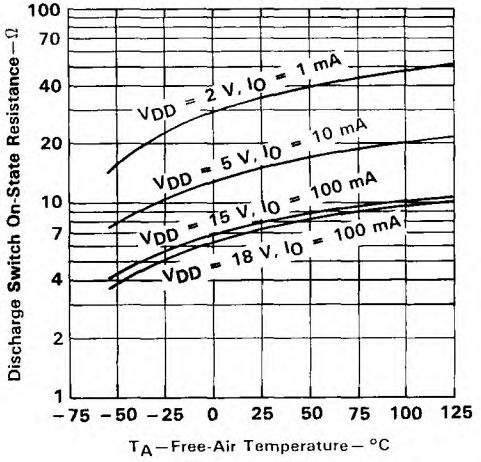
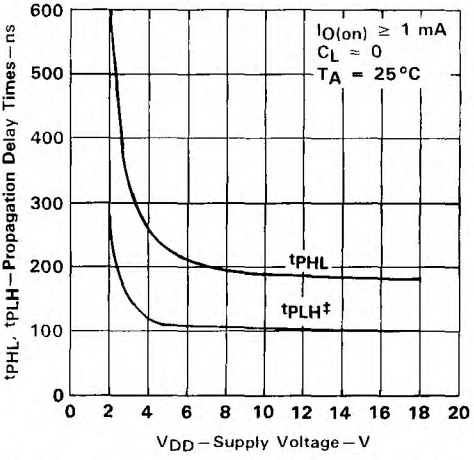


FIGURE 1

PROPAGATION DELAY TIMES
TO DISCHARGE OUTPUT
FROM TRIGGER AND THRESHOLD
SHORTED TOGETHER
vs
SUPPLY VOLTAGE



‡The effects of the load resistance on these values must be taken into account separately.

FIGURE 2

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TYPICAL APPLICATION DATA

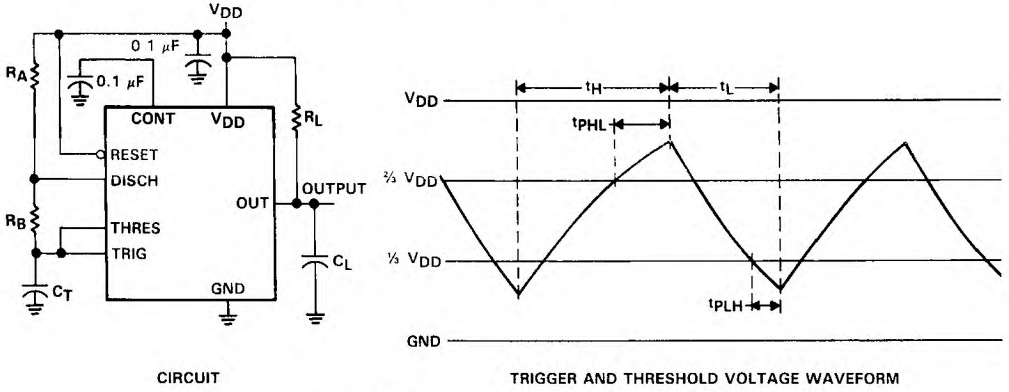


FIGURE 3. ASTABLE OPERATION

Connecting the trigger input to the threshold input, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the trigger voltage level (approximately $0.67V_{DD}$) and then discharges through R_B only to the value of the threshold voltage level (approximately $0.33V_{DD}$). The output is high during the charging cycle (t_H) and low during the discharge cycle (t_L). The duty cycle is controlled by the values of R_A, R_B, and C_T, as shown in the equations below.

$$t_H \approx C_T (R_A + R_B) \ln 2 \qquad (\ln 2 = 0.693)$$

$$t_L \approx C_T R_B \ln 2$$

$$\text{Period} = t_H + t_L \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-μF capacitor at the control pin in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay from the trigger and threshold inputs to the discharge output. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the discharge output resistance r_{on} adds to R_B to provide another source of error in the calculation when R_B is very low or r_{on} is very high.

The equations below provide better agreement with measured values.

$$t_H = C_T (R_A + R_B) \ln\left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})}\right)\right] + t_{PHL}$$

$$t_L = C_T (R_B + r_{on}) \ln\left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)}\right)\right] + t_{PLH}$$

The preceding equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln 2 at low frequencies and ln 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\frac{t_H}{t_H + t_L}$ will require that $\frac{t_H}{t_L} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

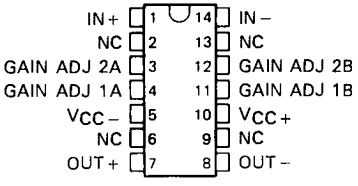
In monostable applications, the trip point of the trigger input can be set by a voltage applied to the control pin. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500 μA bias provides good results.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D922, NOVEMBER 1970—REVISED APRIL 1988

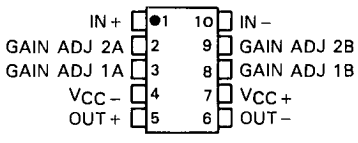
- 200-MHz Bandwidth
- 250-kΩ Input Resistance
- Selectable Nominal Amplification of 10, 100, or 400
- No Frequency Compensation Required
- Designed to be Interchangeable with Fairchild μA733M and μA733C

uA733M . . . J DUAL-IN-LINE PACKAGE
uA733C . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

UA733M . . . U FLAT PACKAGE
(TOP VIEW)



description

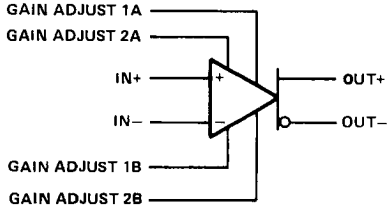
The uA733 is a monolithic two-stage video amplifier with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between 1A and 1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

symbol



The uA733M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA733C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA733M	UA733C	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differentiel input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package			°C

NOTE 1. All voltage values, except differential input voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	N/A	N/A	500 mW	N/A
J (uA733M)	500 mW	11.0 mW/°C	104°C	500 mW	275 mW
N	500 mW	N/A	N/A	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	135 mW

electrical characteristics, $V_{CC+} = 6$ V, $V_{CC-} = -6$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M MIN	uA733M TYP	uA733M MAX	uA733C MIN	uA733C TYP	uA733C MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{OD} = 1$ V	1		400	500		400	600	V/V
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	$R_S = 50\ \Omega$	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	μA
I_{IB}	Input bias current			Any		9	20		9	30	μA
V_{ICR}	Common-mode input voltage range	1		Any*	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	$V_{OD} \leq 1$ V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	$V_{OD} \leq 1$ V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	$V_{IC} = \pm 1$ V, f ≤ 100 kHz	2	60	86		60	86		dB
			$V_{IC} = \pm 1$ V, f = 5 MHz	2		70			70		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	$\Delta V_{CC+} = \pm 0.5$ V, $\Delta V_{CC-} = \pm 0.5$ V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time	2	$R_S = 50\ \Omega$, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	$R_S = 50\ \Omega$, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, No signal	Any		16	24		16	24	mA

† The gain option is selected as follows:
Gain Option1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

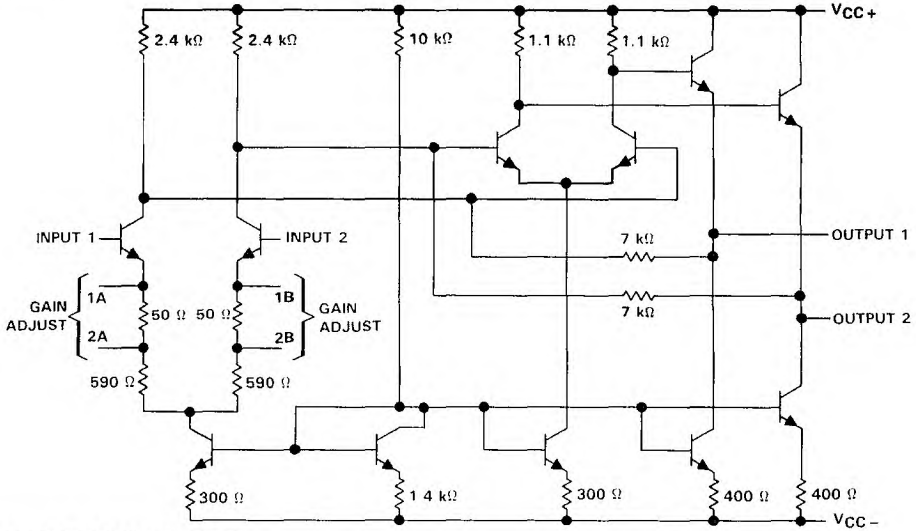
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = −55°C to 125°C for uA733M, 0°C to 70°C for uA733C

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M		uA733C		UNIT
					MIN	MAX	MIN	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1		600			V/V
				2	80	120	80	120	
				3	8	12	8	12	
I_{IO}	Input offset current			Any		5		6	μA
I_{IB}	Input bias current			Any		40		40	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1		±1		V
V_{OO}	Output offset voltage	1		1		1.5		1.5	V
				2 & 3		1.2		1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	2.5		2.8		V
r_i	Input resistance	3	V_{OD} ≤ 1 V	2	8		8		kΩ
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	50		50		dB
			V_{IC} = ±1 V, f = 5 MHz	2					
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50		50		dB
$I_{sink(max)}$	Maximum output sink current			Any	2.2		2.5		mA
I_{CC}	Supply current		No load, No signal	Any		27		27	mA

†The gain option is selected as follows:
Gain Option 1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

schematic



Component values shown are nominal.

4 Special Functions

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage that if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio (k_{SVR}) The absolute value of the ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

Equivalent Input Noise Voltage (V_n) The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents I_{CC1} and I_{CC2}.

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

test circuits

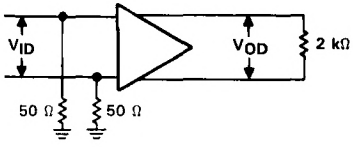


FIGURE 1

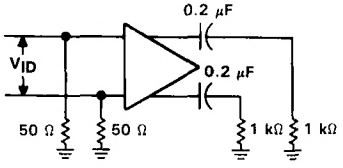


FIGURE 2

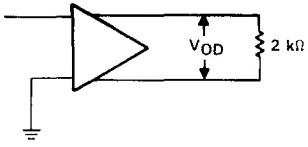


FIGURE 3

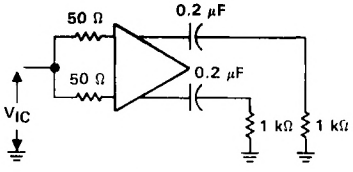


FIGURE 4

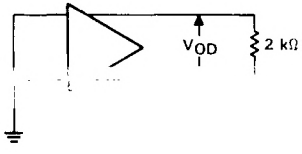
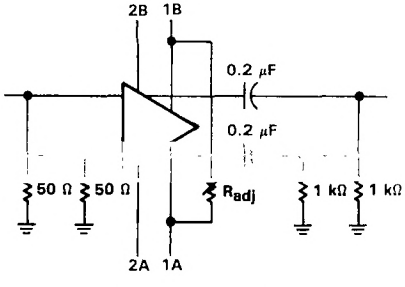


FIGURE 5



VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

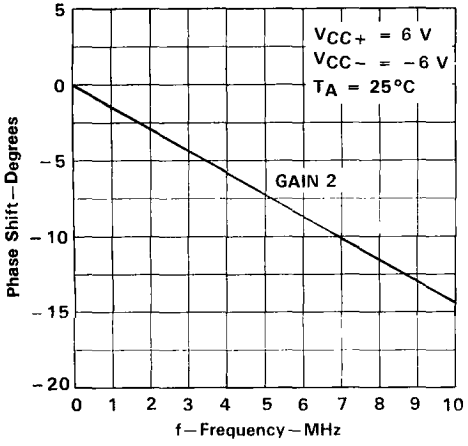


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

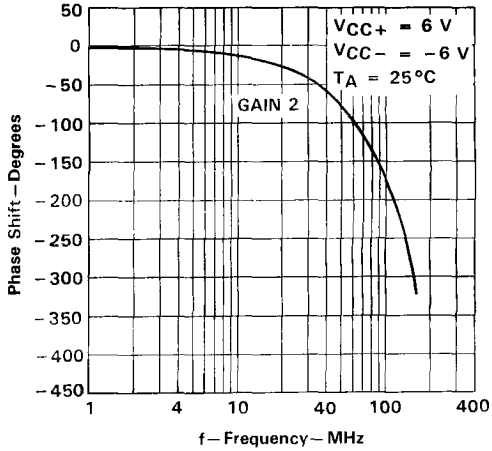


FIGURE 8

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
TEMPERATURE

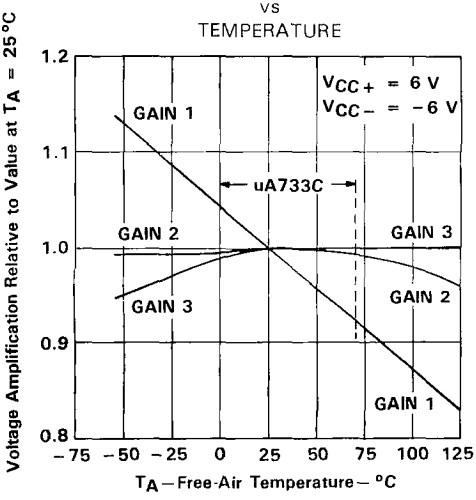


FIGURE 9

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
SUPPLY VOLTAGE

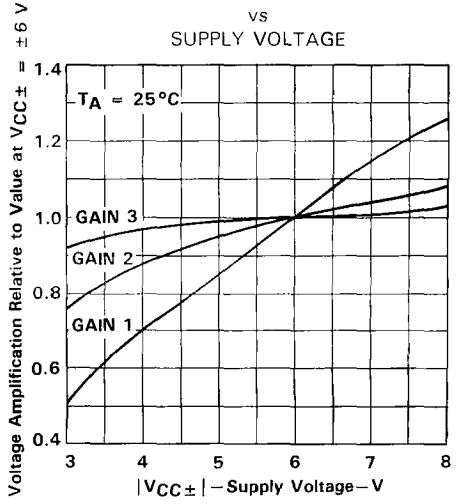


FIGURE 10

4 Special Functions

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TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
RESISTANCE BETWEEN G1A AND G1B

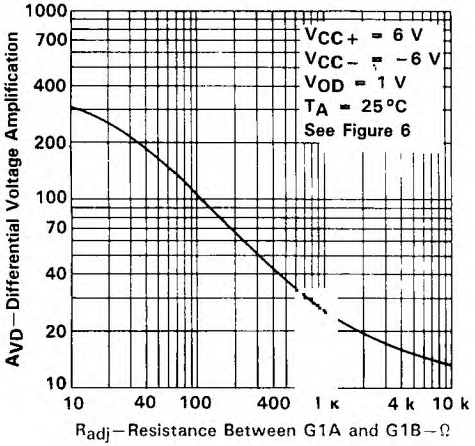

FIGURE 11

SINGLE-ENDED VOLTAGE AMPLIFICATION
vs
FREQUENCY

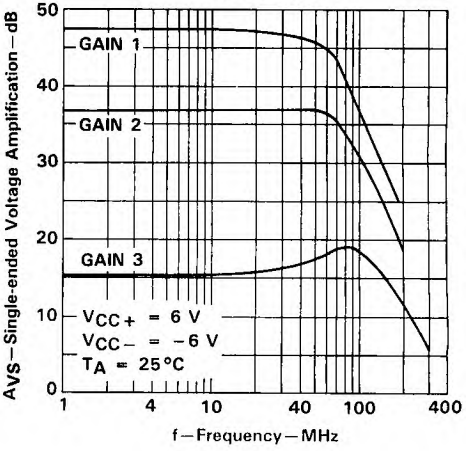

FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

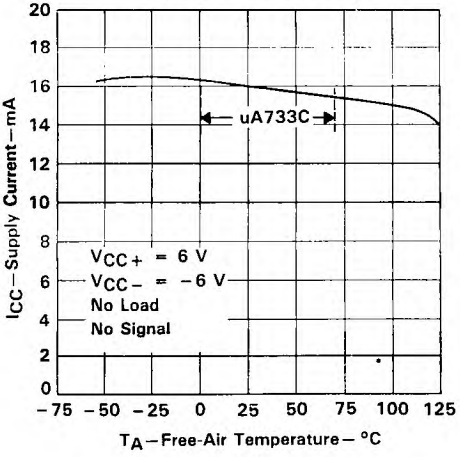

FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

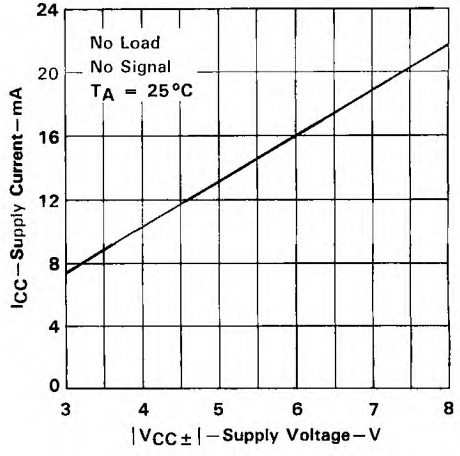

FIGURE 14

4 Special Functions

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

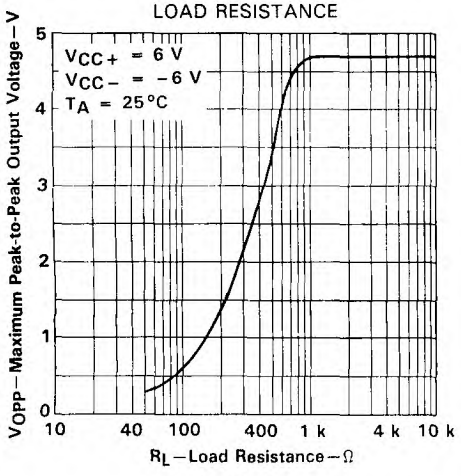

FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

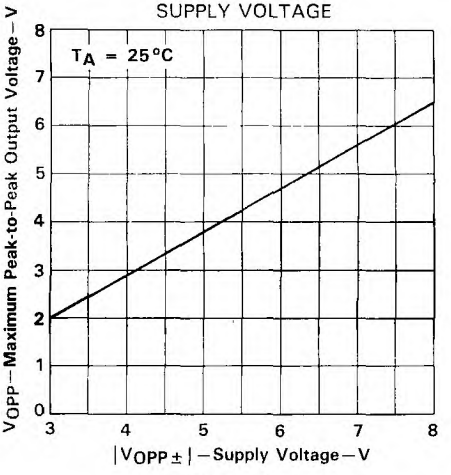

FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

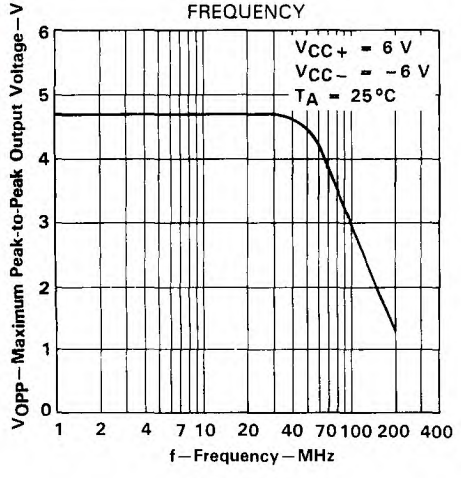

FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

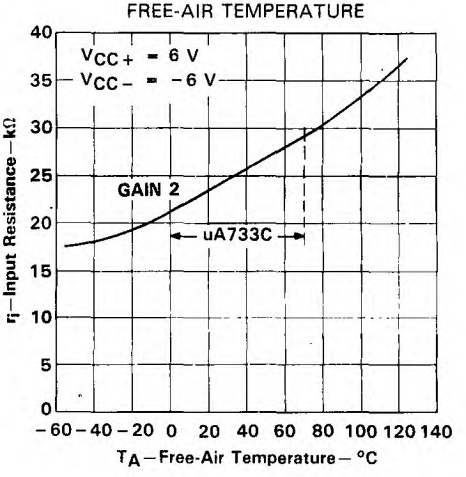

FIGURE 18

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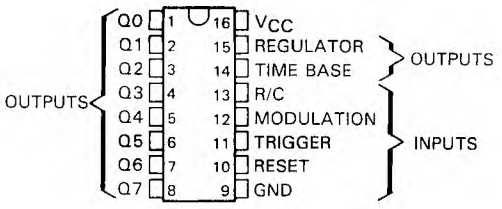
D2442, JUNE 1978 REVISED MAY 1988

- **Accurate Timing from Microseconds to Days**
- **Programmable Delays from 1 Time Constant to 255 Time Constants**
- **Outputs Compatible with TTL and CMOS**
- **Wide Supply-Voltage Range**
- **External Sync and Modulation Capability**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

These circuits consist of a time-base oscillator, and eight-bit counter, a control flip-flop, and a voltage regulator. The frequency of the time-base oscillator is set by the time constant of an external resistor and capacitor at pin 13 and can be synchronized or modulatd by signals applied to the modulation input. The output of the time-base section is applied directly to the input of the counter section and also appears at pin 14 (time base). The time-base pin may be used to monitor the frequency of the oscillator, to provide an output pulse to other circuitry, or (with the time-base section disabled) to drive the counter input from an external source. The counter input is activated on a negative-going transition. The reset input stops the time-base oscillator and sets each binary output, Q0 through Q7, and the time-base output to a TTL high level. After resetting, the trigger input starts the oscillator and all Q outputs go low. Once triggered, the uA2240C will ignore any signals at the trigger input until it is reset.

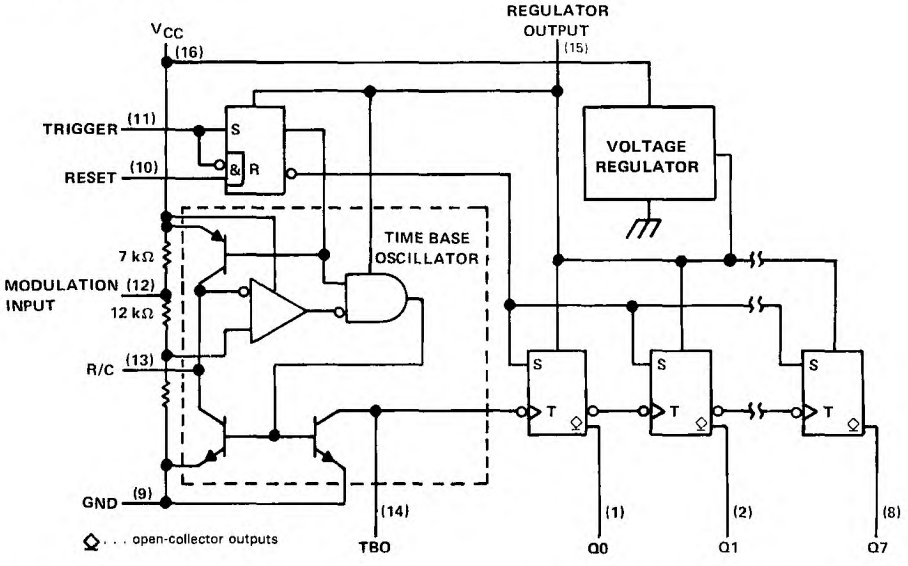
The uA2240C timer/counter may be operated in the free-running mode or with output-signal feedback to the reset input for automatic reset. Two or more binary outputs may be connected together to generate complex pulse patterns, or each output may be used separately to provide eight output frequencies. Using two circuits in cascade can provide precise time delays of up to three years.

The uA2240C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_T MAX at 25°C
DEVICE	PACKAGE SUFFIX		
uA2240C	N	0°C to 70°C	2 V

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Output voltage: Q0 thru Q7 . . . . . 18 V
Output current: Q0 thru Q7 . . . . . 10 mA
Regulator output current . . . . . −5 mA
Continuous dissipation at (or below) 25°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4		14	V
Timing resistor	0.001		10	MΩ
Timing capacitor	0.01		1000	μF
Counter input frequency (Pin 14)		1.5		MHz
Pull-up resistor, time-base output		20		kΩ
Trigger and reset input pulse voltage	2	3		V
Trigger and reset input pulse duration	2			μs
External clock input pulse voltage	3			V
External clock input pulse duration	1			μs

NOTE 2: For operation with $V_{CC} \leq 4.5$ V, short regulator output to V_{CC}.

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electrical characteristics at 25°C free-air temperature

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator output voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	3.9	4.4		V
	2	V_{CC} = 15 V, Trigger and reset open or grounded	5.8	6.3	6.8	
Modulation input open circuit voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	2.8	3.5	4.2	V
		V_{CC} = 15 V, Trigger and reset open or grounded		10.5		
Trigger threshold voltage	1	V_{CC} = 5 V, Reset at 0 V		1.4	2	V
High-level trigger current	1	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V		10		μA
Reset threshold voltage	1	V_{CC} = 5 V, Trigger at 0 V		1.4	2	V
High-level reset current	1	V_{CC} = 5 V, Trigger at 0 V		10		μA
Counter input (time base) threshold voltage	2	V_{CC} = 5 V, Trigger and reset open or grounded	1	1.4		V
Low-level output current, Q0 thru Q7	2	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V, V_{OL} < 0.4 V	2	4		mA
High-level output current, Q0 thru Q7	2	V_{OH} = 15 V, Reset at 2 V, Trigger at 0 V		0.01	15	μA
Supply current	1	V_{CC} = 5 V, Trigger at 0 V, Reset at 5 V		4	7	mA
	1	V_{CC} = 15 V, Trigger at 0 V, Reset at 5 V		13	18	
	3	V+ = 4 V		1.5		

operating characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Initial error of time base‡	1	V_{CC} = 5 V, Trigger at 5 V, Reset at 0 V			±0.5	±5	%
Temperature coefficient of time-base period	1	T_A = 0°C to 70°C	V_{CC} = 5 V		−200		ppm/°C
			V_{CC} = 15 V		−80		
Supply voltage sensitivity of time-base period	1	V_{CC} ≥ 8 V			0.05	0.1	%/V
Time-base output frequency	1	V_{CC} = 5 V, R = MIN, C = MIN			130		kHz
Propagation delay time		see Note 3	From trigger input		1		μs
			From reset input		0.8		
Output rise time	2	R_L = 3 kΩ, C_L = 10 pF	Q0 thru Q7		100		ns
Output fall time					100		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This is the time-base period error due only to the uA2240C and expressed as a percentage of nominal (1.00 RC).
NOTE 3: Propagation delay time is measured from the 50% point on the leading edge of an input pulse to the 50% point on the leading edge of the resulting change of state at Q0.

PARAMETER MEASUREMENT INFORMATION

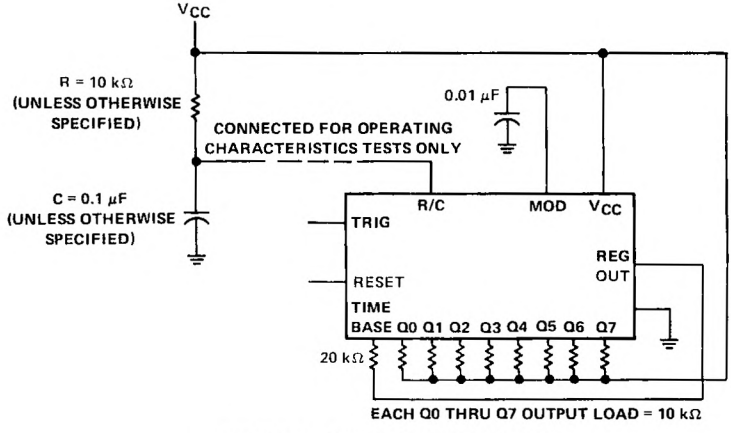

FIGURE 1. GENERAL TEST CIRCUIT

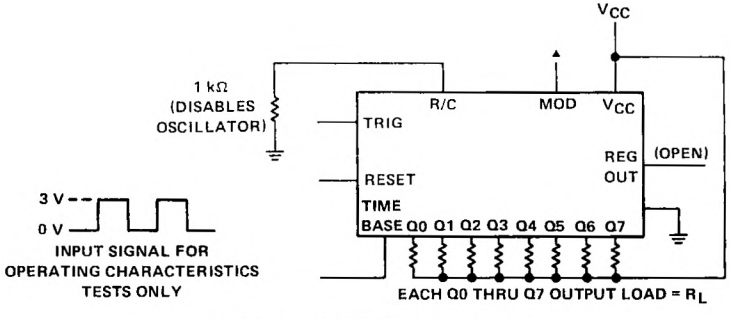

FIGURE 2. COUNTER TEST CIRCUIT

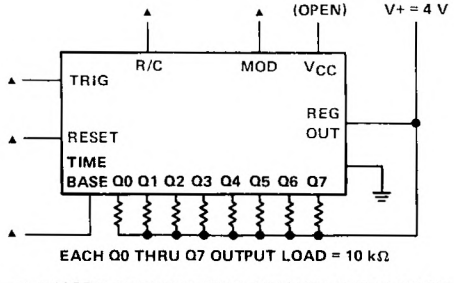

FIGURE 3. REDUCED-POWER TEST CIRCUIT (TIME BASE DISABLED)

▲These connections may be open or grounded for this test.

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TYPICAL CHARACTERISTICS

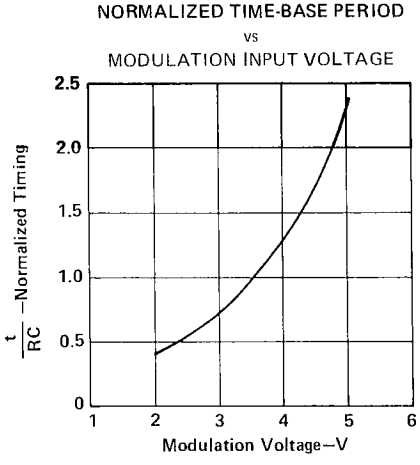

FIGURE 4

TYPICAL APPLICATION INFORMATION

Figure 5 shows voltage waveforms for typical operation of the uA2240C. If both reset and trigger inputs are low during power-up, the timer/counter will be in a reset state with all binary (Q) outputs high and the oscillator stopped. In this state, a high level on the trigger input starts the time-base oscillator. The initial negative-going pulse from the oscillator sets the Q outputs to low logic levels at the beginning of the first time-base period. The uA2240C will ignore any further signals at the trigger input until after a reset signal is applied to the reset input. With the trigger input low, a high level at the reset input will set Q outputs high and stop the time-base oscillator. If the reset signal occurs while the trigger input is high, the reset is ignored. If the reset input remains high when the trigger input goes low, the uA2240C will reset.

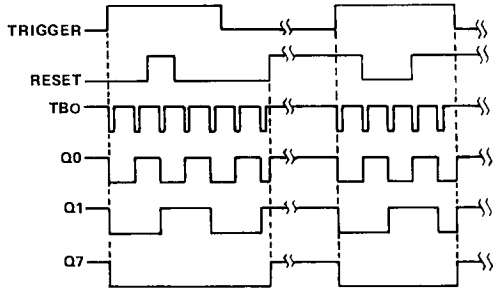

FIGURE 5. TIMING DIAGRAM OF OUTPUT WAVEFORMS

TYPICAL APPLICATION INFORMATION

In monostable applications of the uA2240C, one or more of the binary outputs will be connected to the reset terminal as shown in Figure 6. The binary outputs are open-collector stages that can be connected together to a common pull-up resistor to provide a "wired-OR" function. The combined output will be low as long as any one of the outputs is low. This type of arrangement can be used for time delays that are integer multiples of the time-base period. For example, if Q5 ($2^5 = 32$) only is connected to the reset input, every trigger pulse will generate a 32-period active-low output. Similarly, if Q0, Q4, and Q5 are connected to reset, each trigger pulse creates a 49-period delay.

In astable operation, the uA2240C will free-run from the time it is triggered until it receives an external reset signal.

The period of the time-base oscillator is equal to the RC time constant of an external resistor and capacitor connected as shown in Figure 6 when the modulation input is open (approximately 3.5 V internal, see Figure 4). Under conditions of high supply voltage ($V_{CC} > 7$ V) and low value of timing capacitor ($C < 0.1\ \mu F$), the pulse duration of the time-base oscillator may be too short to properly trigger the counters. This situation can be corrected by adding a 300-pF capacitor between the time-base output and ground. The time-base output (TBO) is an open-collector output that requires a 20-kΩ pull-up resistor to Pin 15 for proper operation. The time-base pin may also be used as an input to the counters for an external time-base or as an active-low inhibit input to interrupt counting without resetting.

The modulation input varies the ratio of the time-base period to the RC time constant as a function of the dc bias voltage (see Figure 4). It can also be used to synchronize the timer/counter to an external clock or sync signal.

The regulator output is used internally to drive the binary counters and the control logic. This terminal can also be used to supply voltage to additional uA2240C devices to minimize power dissipation when several timer circuits are cascaded. For circuit operation with an external clock, the regulator output can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time base, Pin 15 should be shorted to Pin 16.

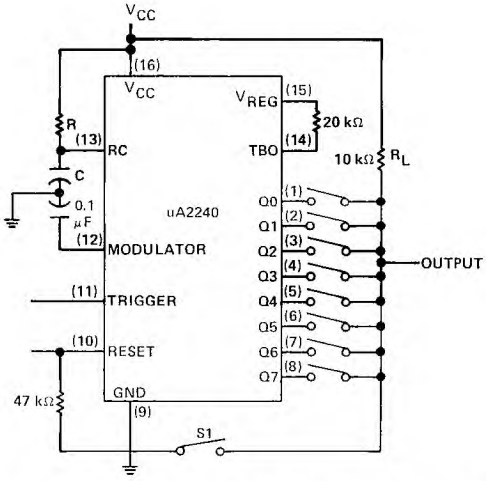

FIGURE 6. BASIC CONNECTIONS FOR TIMING APPLICATIONS

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